
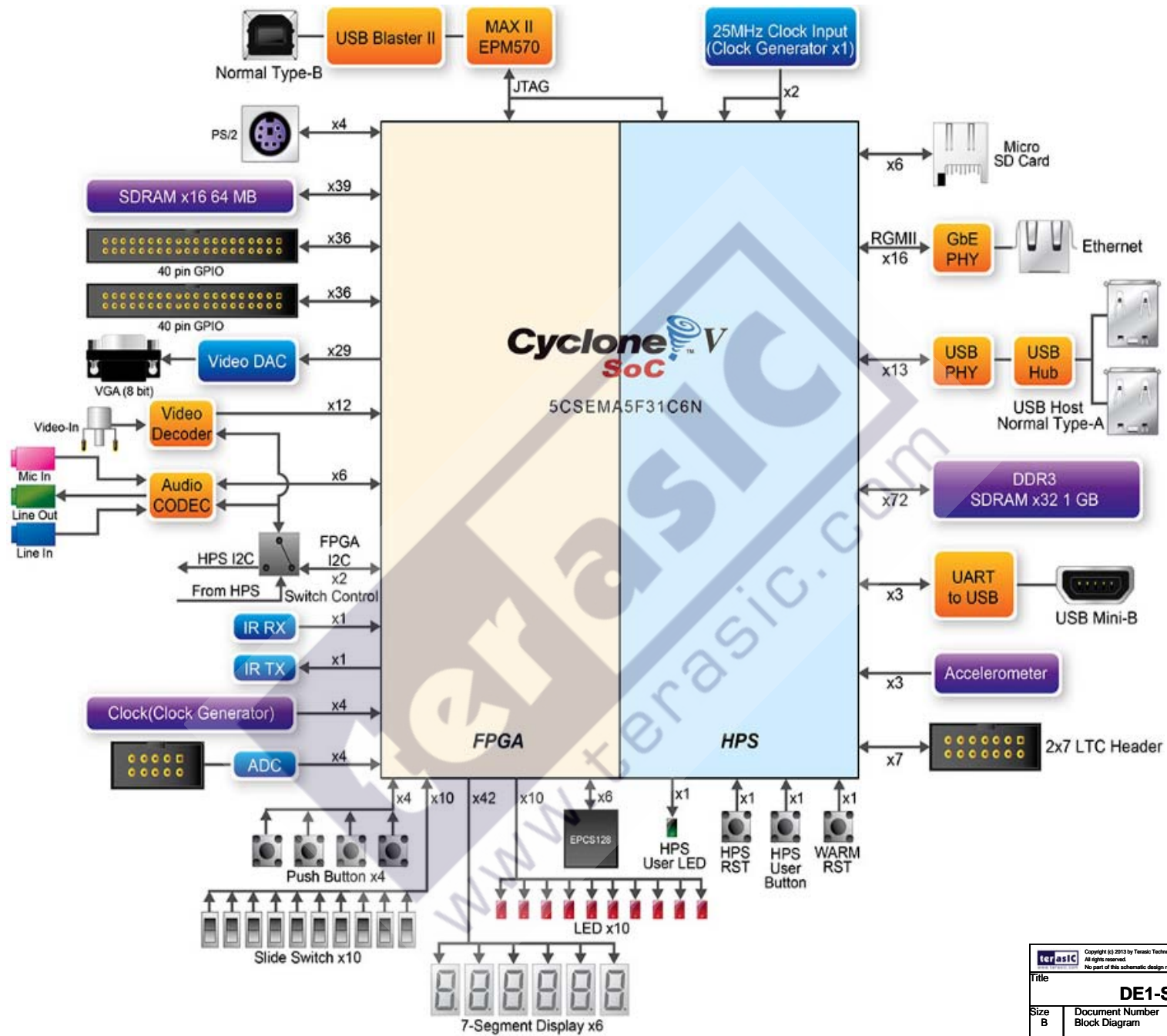


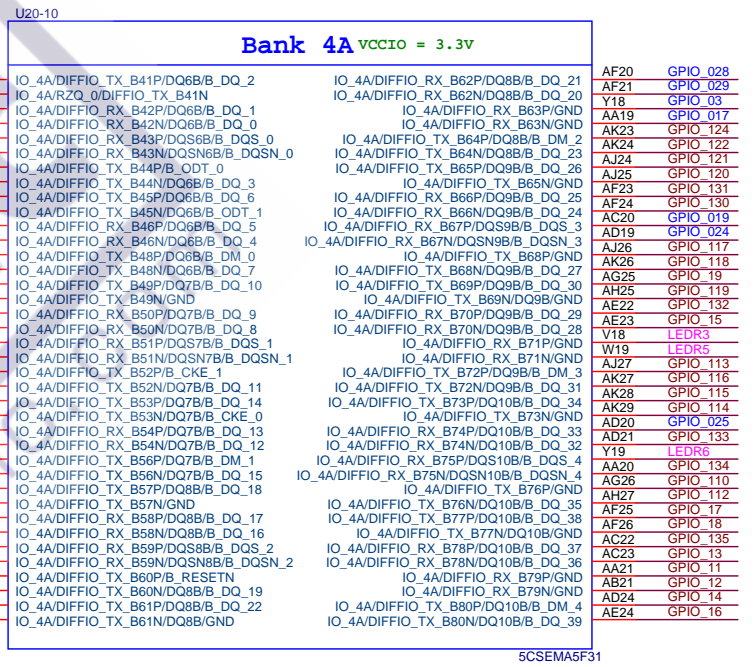
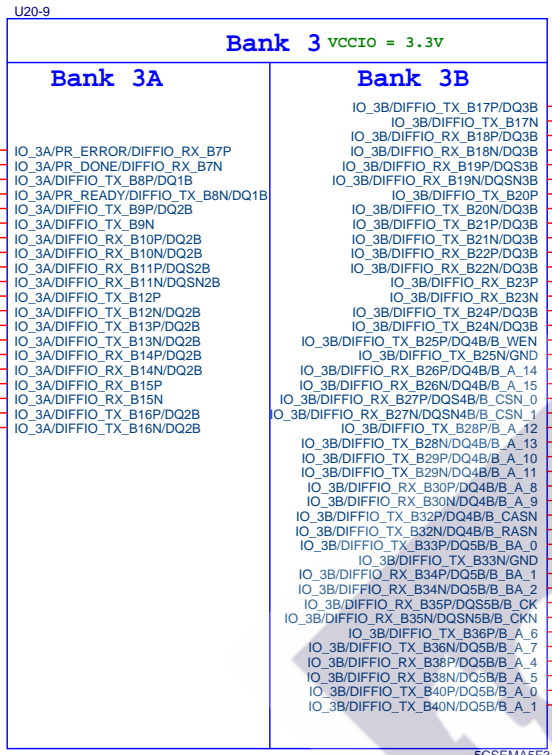
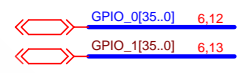
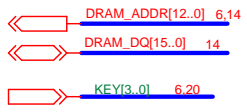
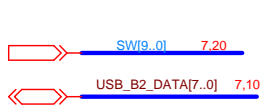
ALTERA Cyclone V SoC Development & Education Board (DE1-SoC)

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6	FPGA Clocks, GND	21	ADC, PS2, IR Tx, IR Rx
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8	FPGA Decoupling	23	1 Gigabit Ethernet
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15	HPS DDR3 SDRAM	30	Power - 1.2V, 1.8V, DDR3 VREF, DDR3 VTT

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Title		
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Size	Document Number	Rev
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Title		
DE1-SoC Board		
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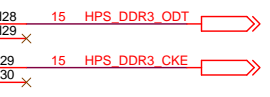
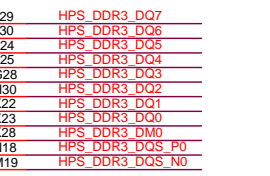
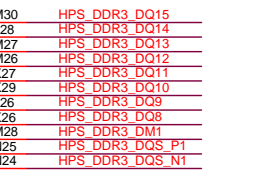
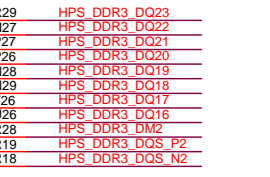
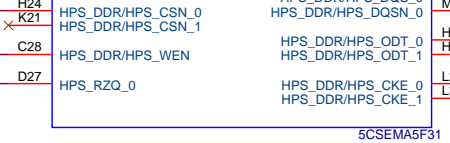
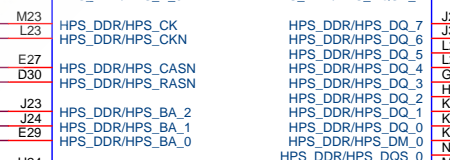
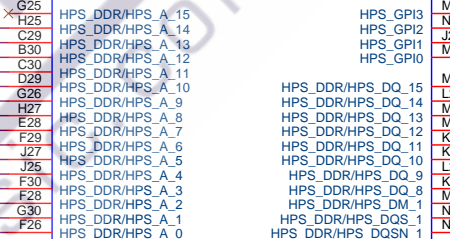
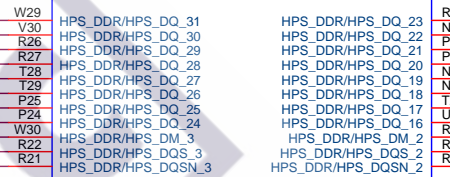
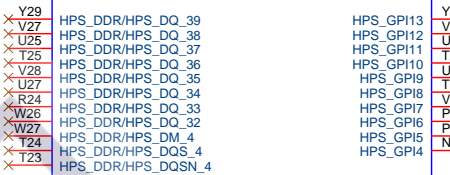
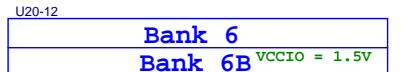
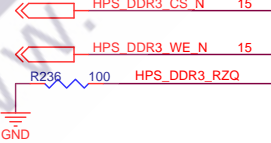
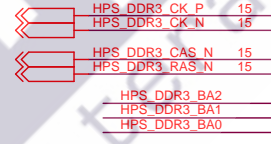
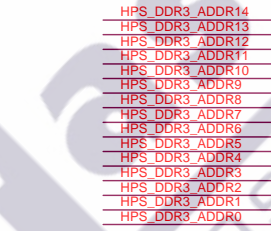
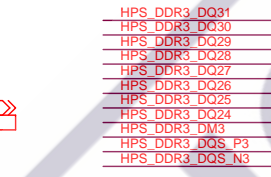
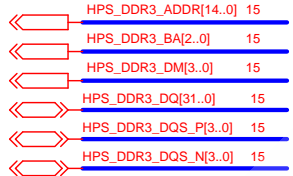
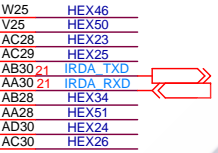
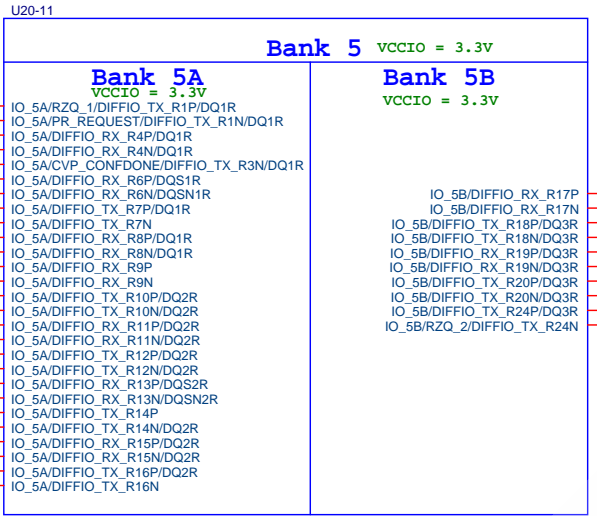
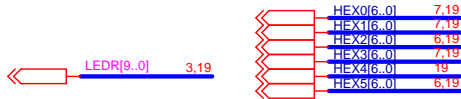
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DE1-SoC Board

Document Number: FPGA BANK 3, BANK 4

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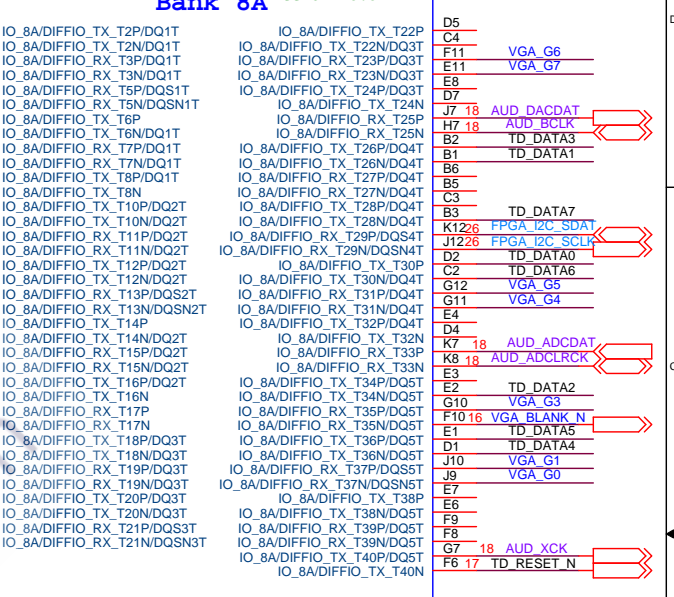
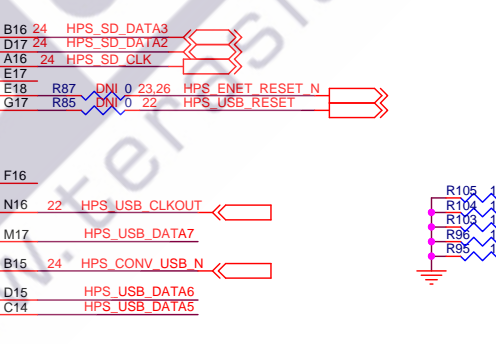
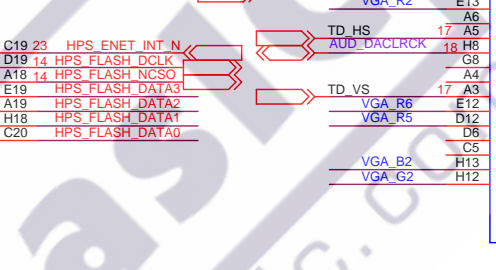
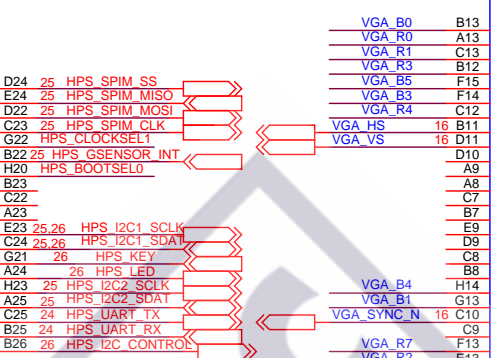
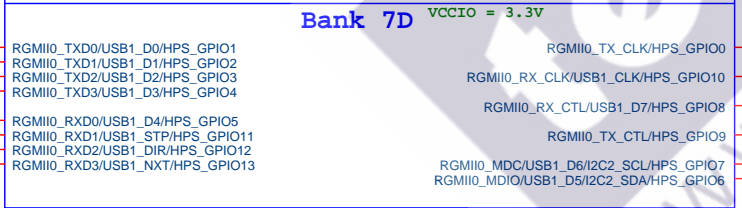
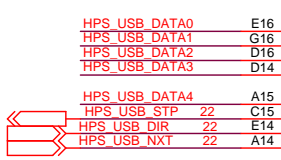
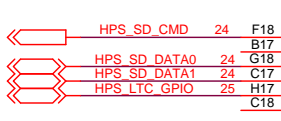
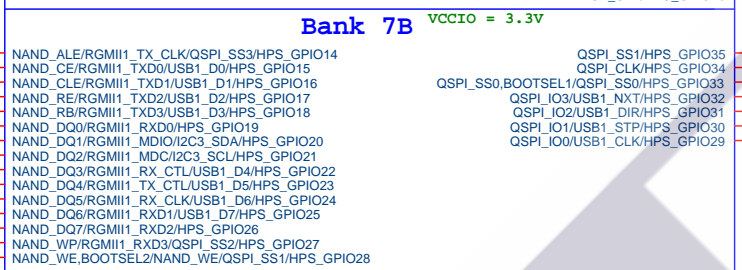
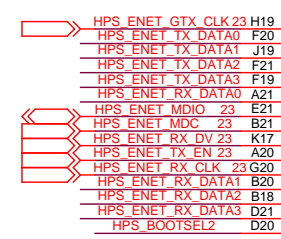
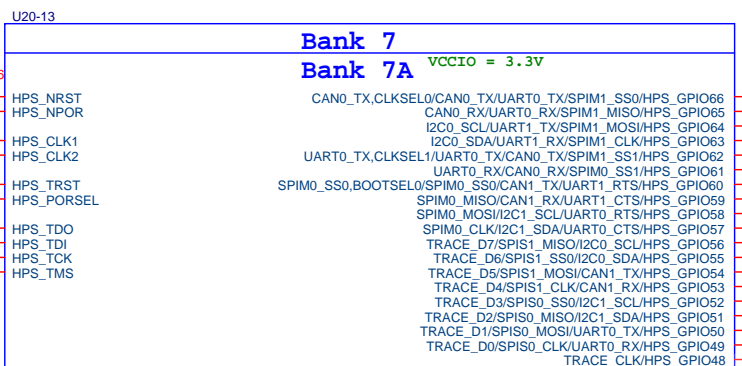
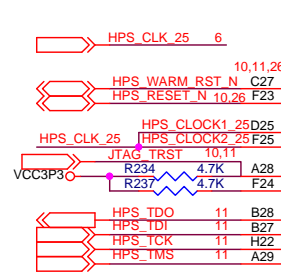


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Title: **DE1-SoC Board**

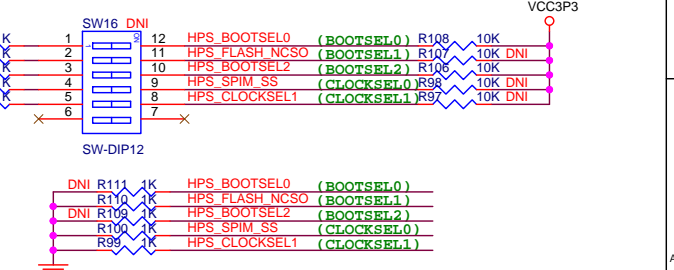
Size B Document Number: **FPGA BANK 5, BANK 6** Rev F

Date: **Thursday, November 20, 2014** Sheet 4 of 30

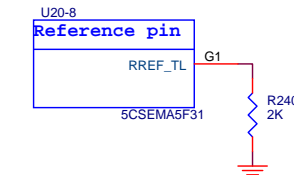
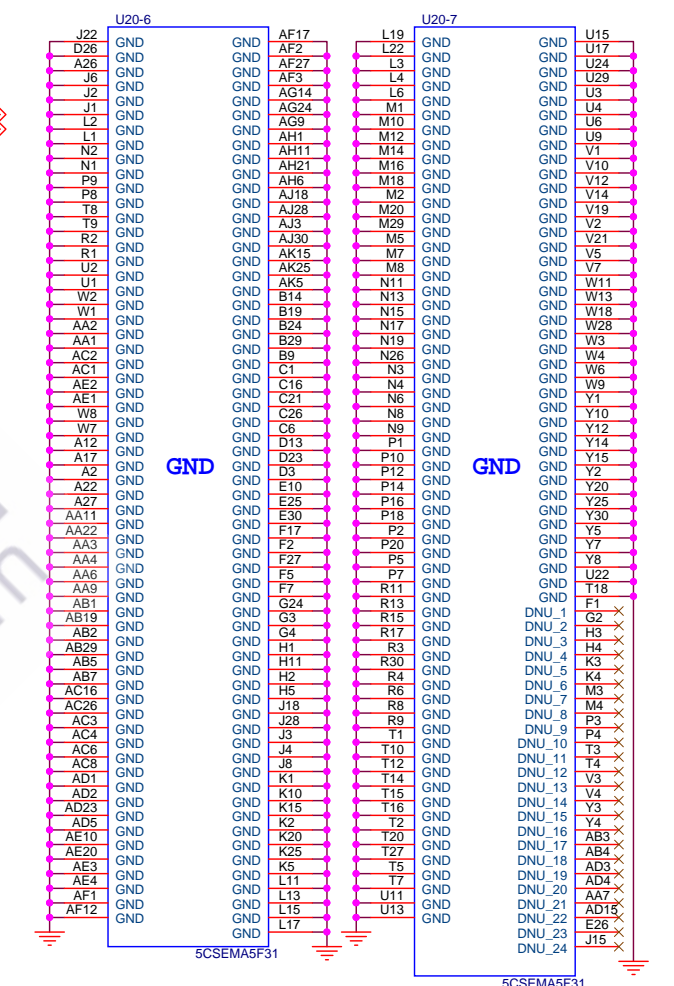
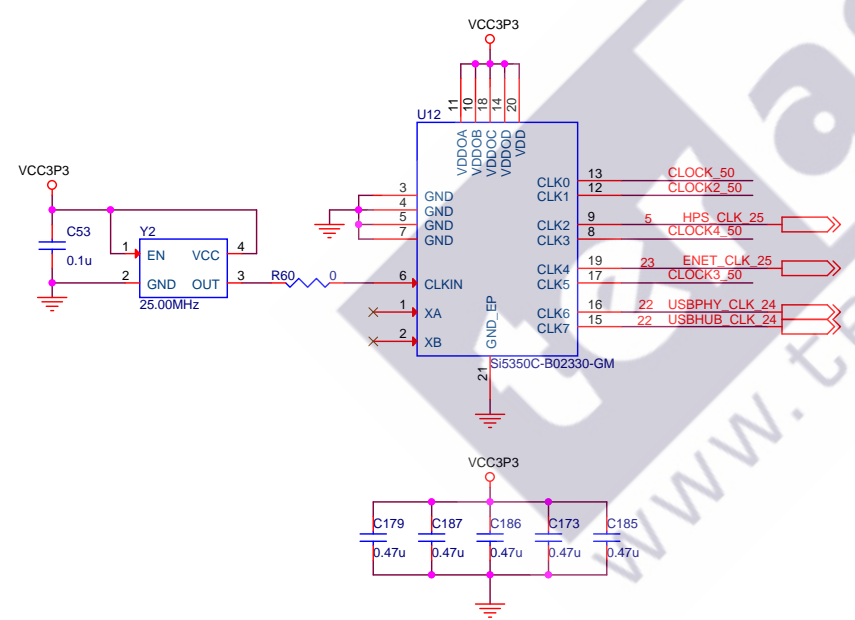
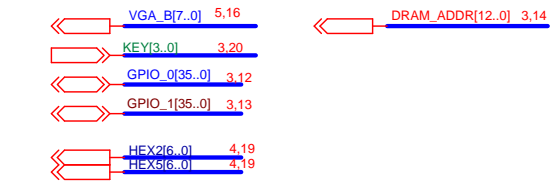
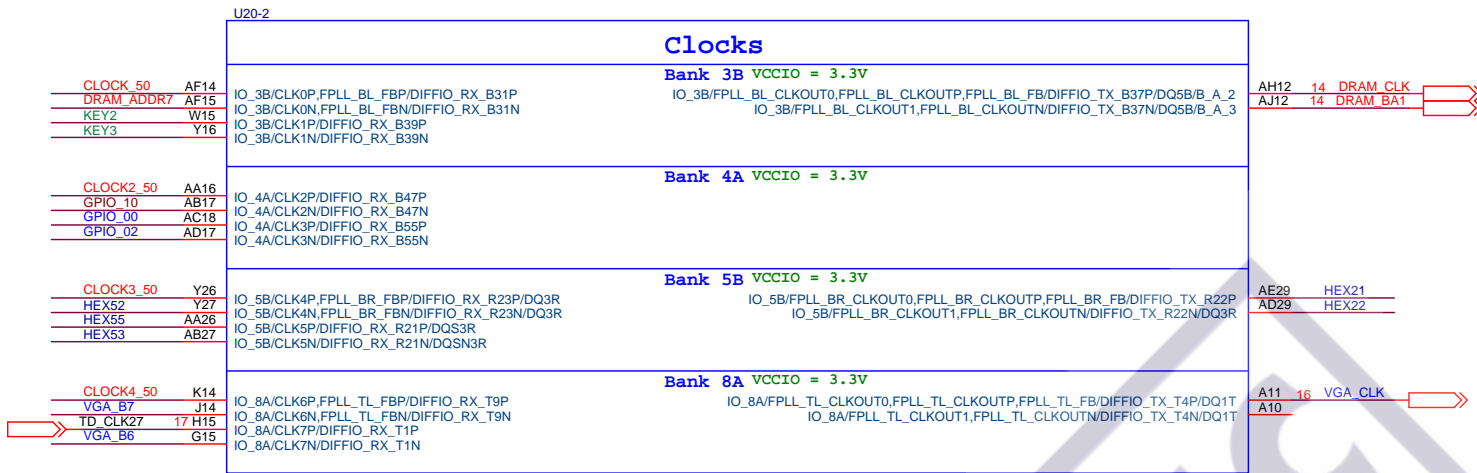


5CSEMA5F31

Default Setting: BOOTSEL[2:0]=101 (Boot from SD CARD)
 CLKSEL[1:0]=0



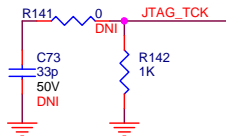
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DE1-SoC Board		
Size B	Document Number FPGA BANK 7, BANK 8	Rev F
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terasic		
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Title: DE1-SoC Board		
Size: B	Document Number: FPGA Clocks & GND	Rev: F
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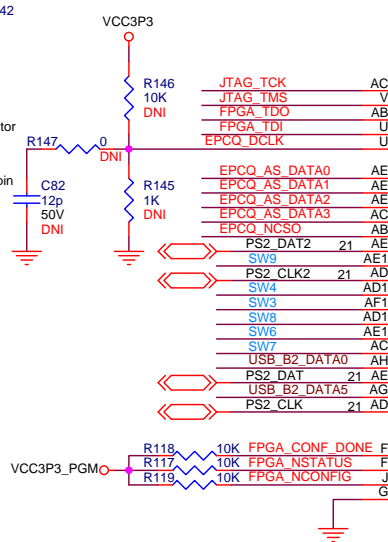
USB Blaster

- FPGA TDI 11
- JTAG TMS 11
- JTAG TCK 11
- FPGA TDO 11



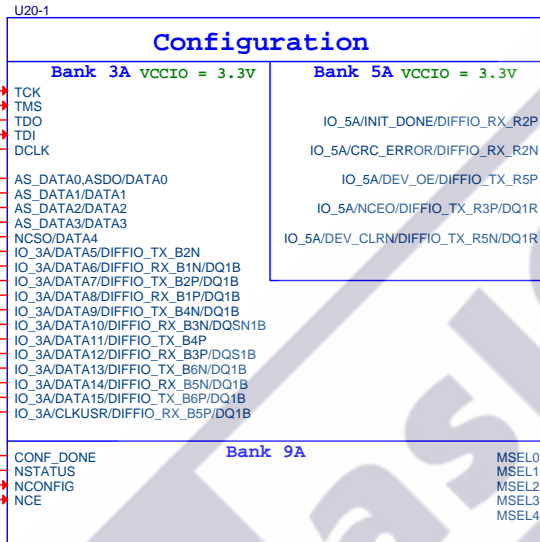
Design Note:
Optional termination resistor for DCLK

CAD Note:
Place near FPGA DCLK pin

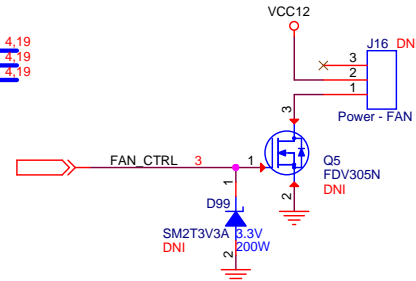


- FPGA NCONFIG 10
- FPGA_CONF_DONE 10

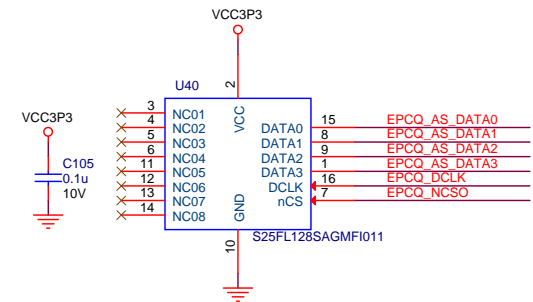
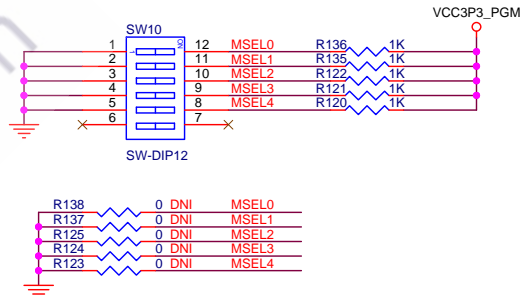
- USB_B2_DATA[7..0] 3,10
- SW[9..0] 3,20



- HEX0[6..0] 4,19
- HEX1[6..0] 4,19
- HEX3[6..0] 4,19

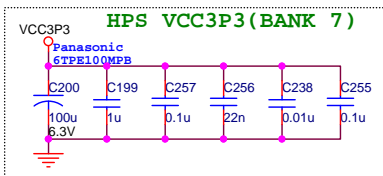
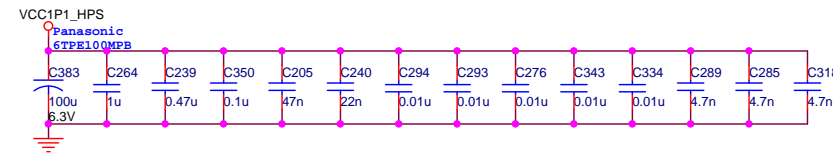
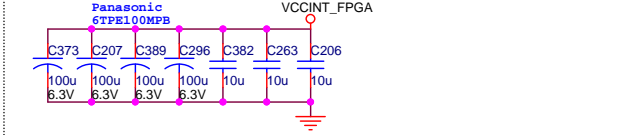
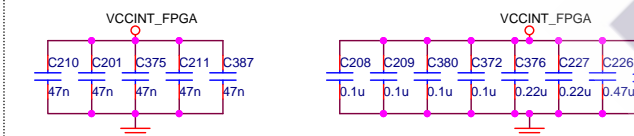
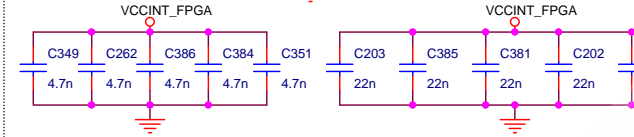
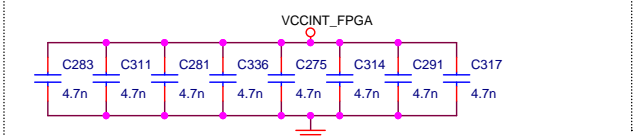
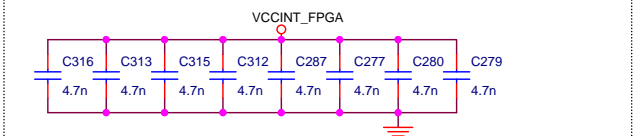
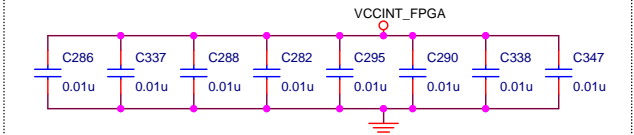
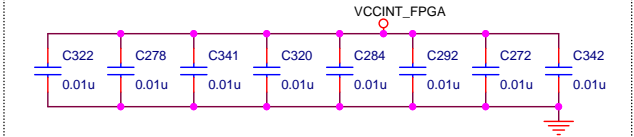
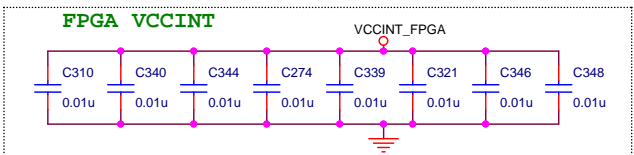


Fix MSEL[4:0]=10010 in AS Fast Mode

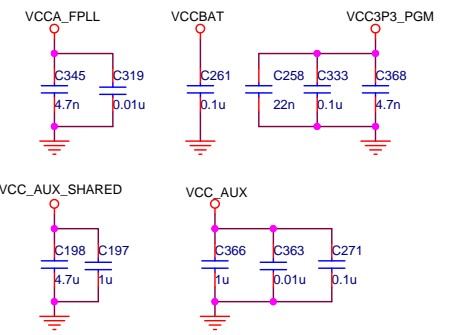
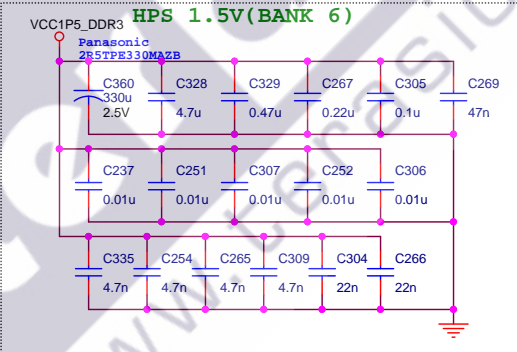
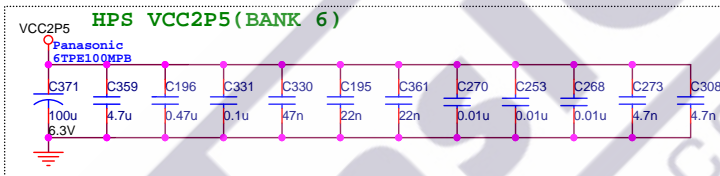
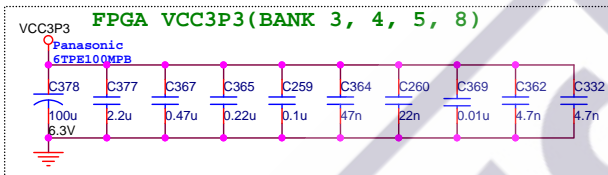


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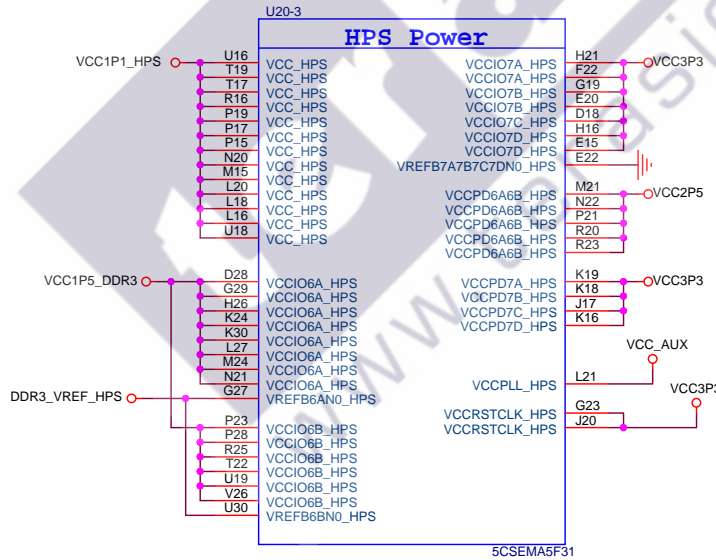
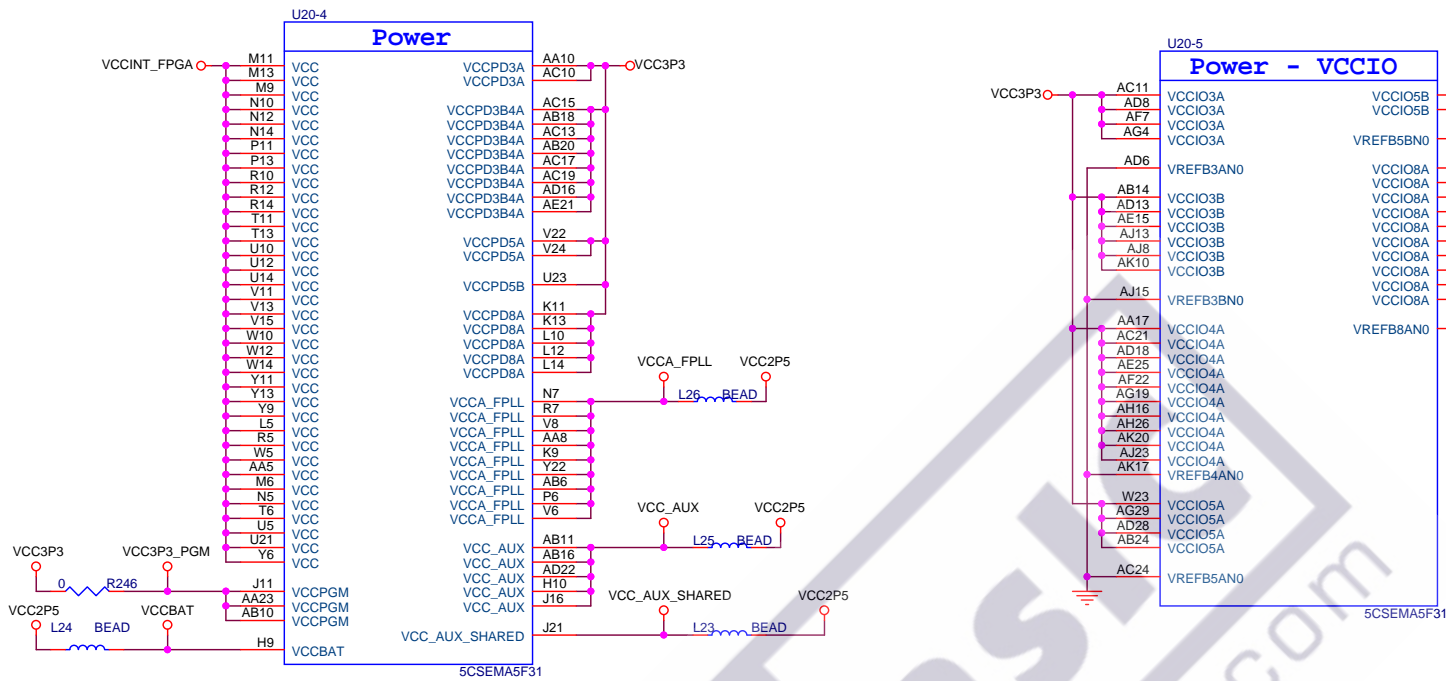
DE1-SoC Board		
Size B	Document Number FPGA Configuration	Rev F
Date:	Thursday, November 20, 2014	Sheet 7 of 30




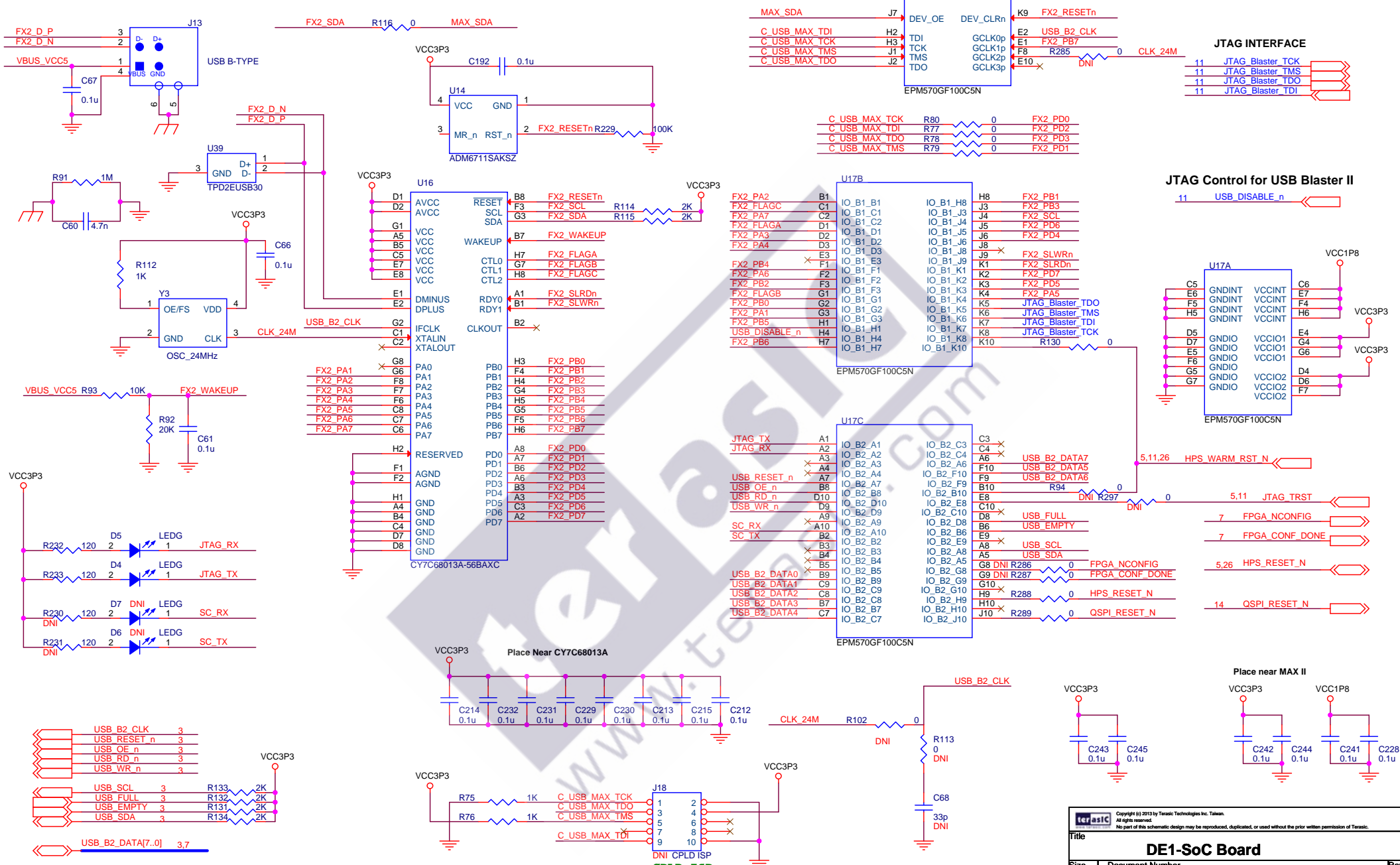
Place C394 close to J20/G23 pin



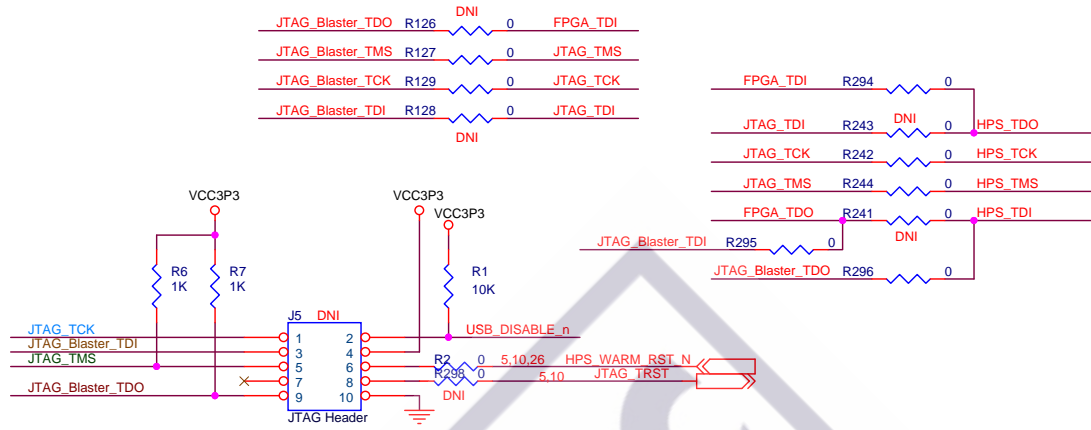
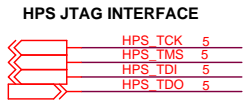
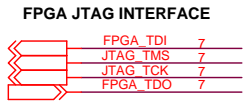
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Title DE1-SoC Board		
Size B	Document Number FPGA Decoupling	Rev F
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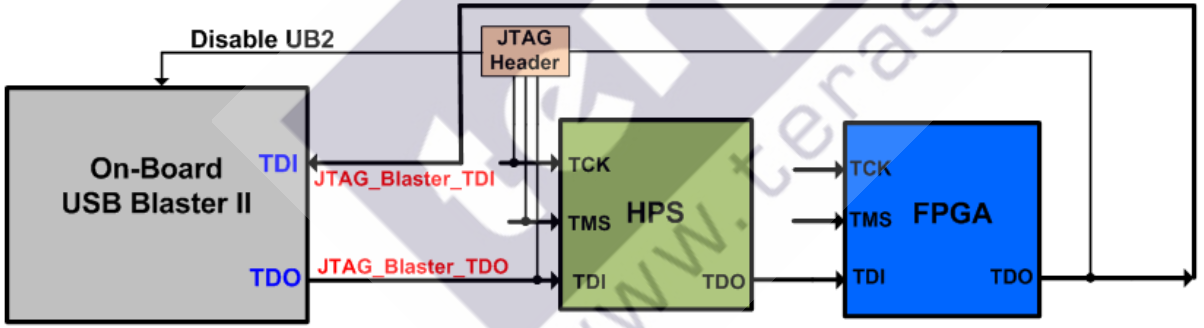
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Title	
DE1-SoC Board	
Size	Document Number
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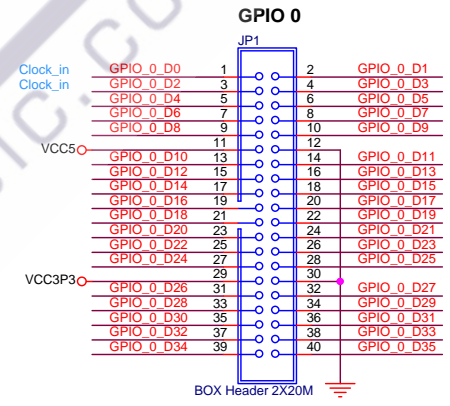
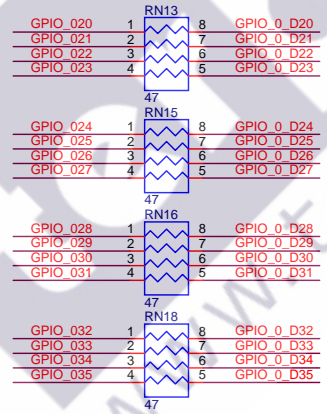
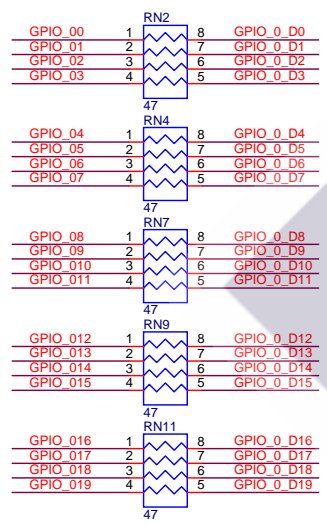
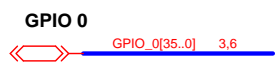
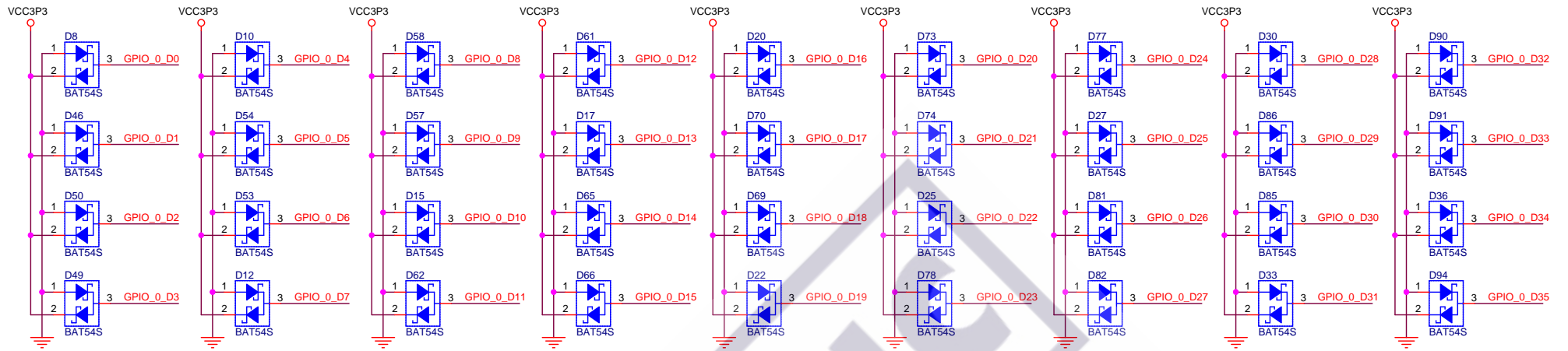


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JTAG Chain



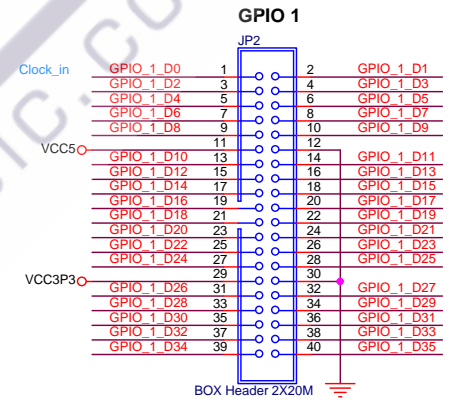
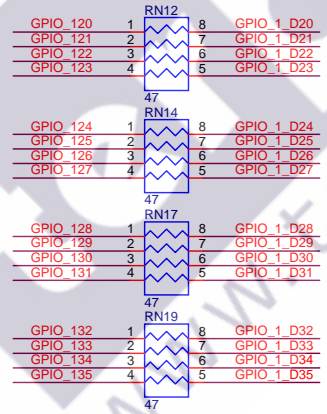
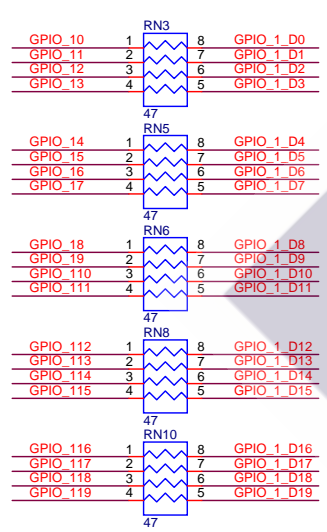
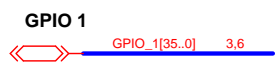
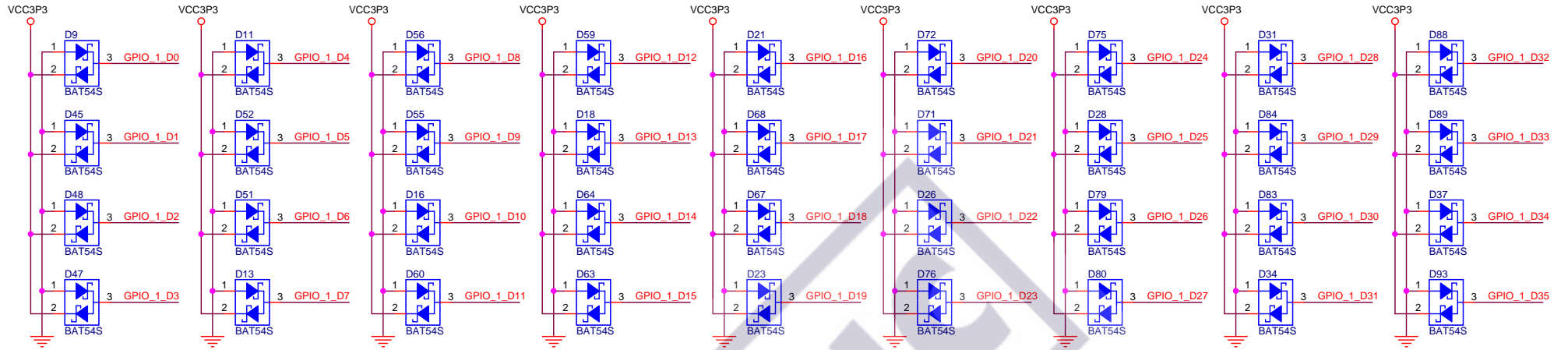


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Title DE1-SoC Board

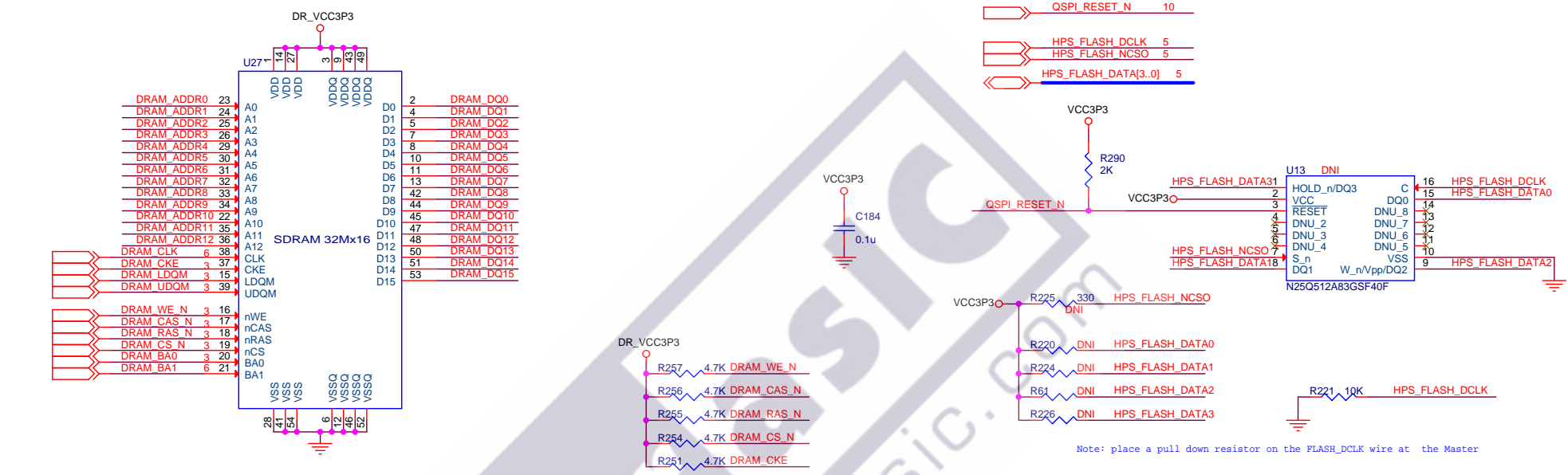
Size B	Document Number GPIO 0	Rev F
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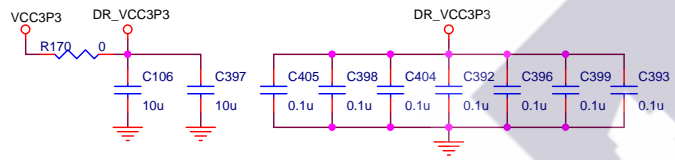


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Title		
DE1-SoC Board		
Size B	Document Number	Rev F
GPIO 1		
Date:	Thursday, November 20, 2014	Sheet 13 of 30

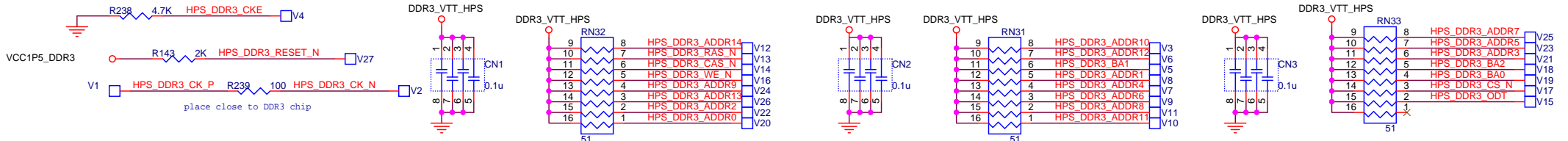
DRAM_DQ[15..0] 3
 DRAM_ADDR[12..0] 3,6



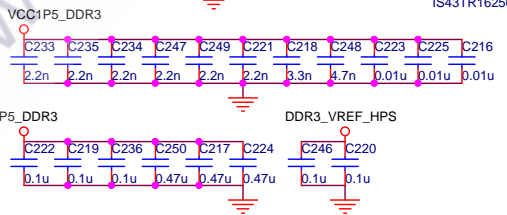
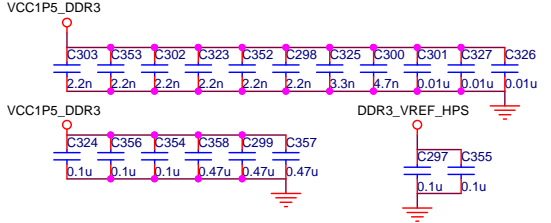
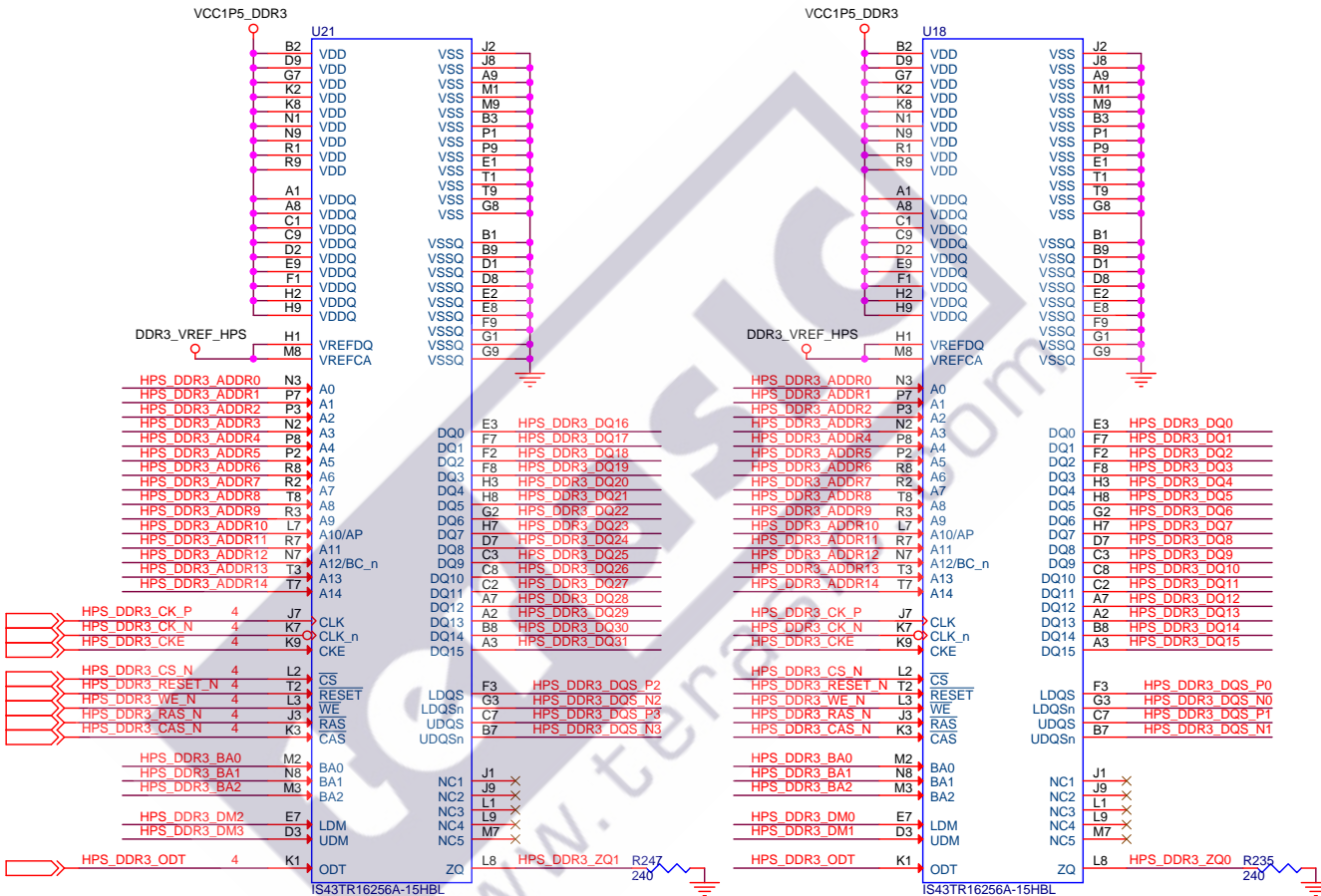
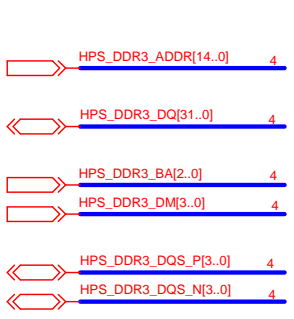
Note: place a pull down resistor on the FLASH_DCLK wire at the Master



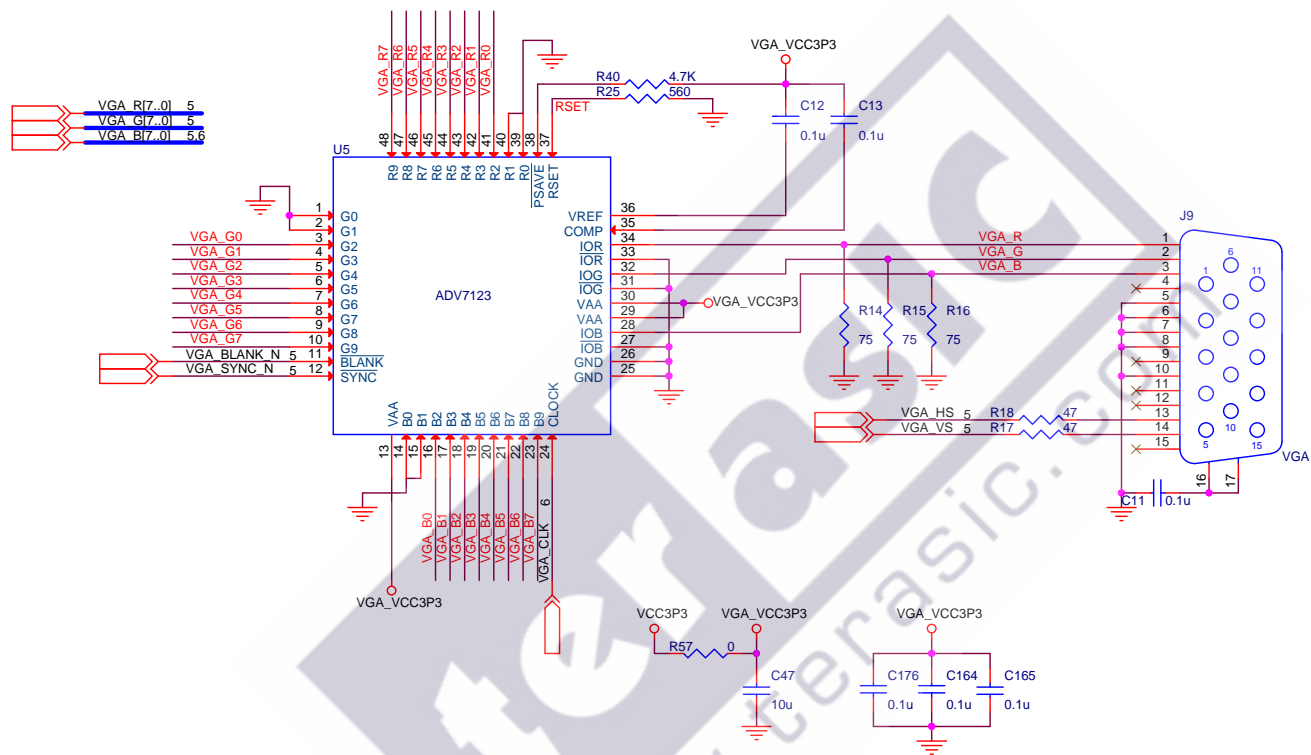
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Title		
DE1-SoC Board		
Size B	Document Number SDRAM & HPS QSPI Flash	Rev F
Date:	Thursday, November 20, 2014	Sheet 14 of 30

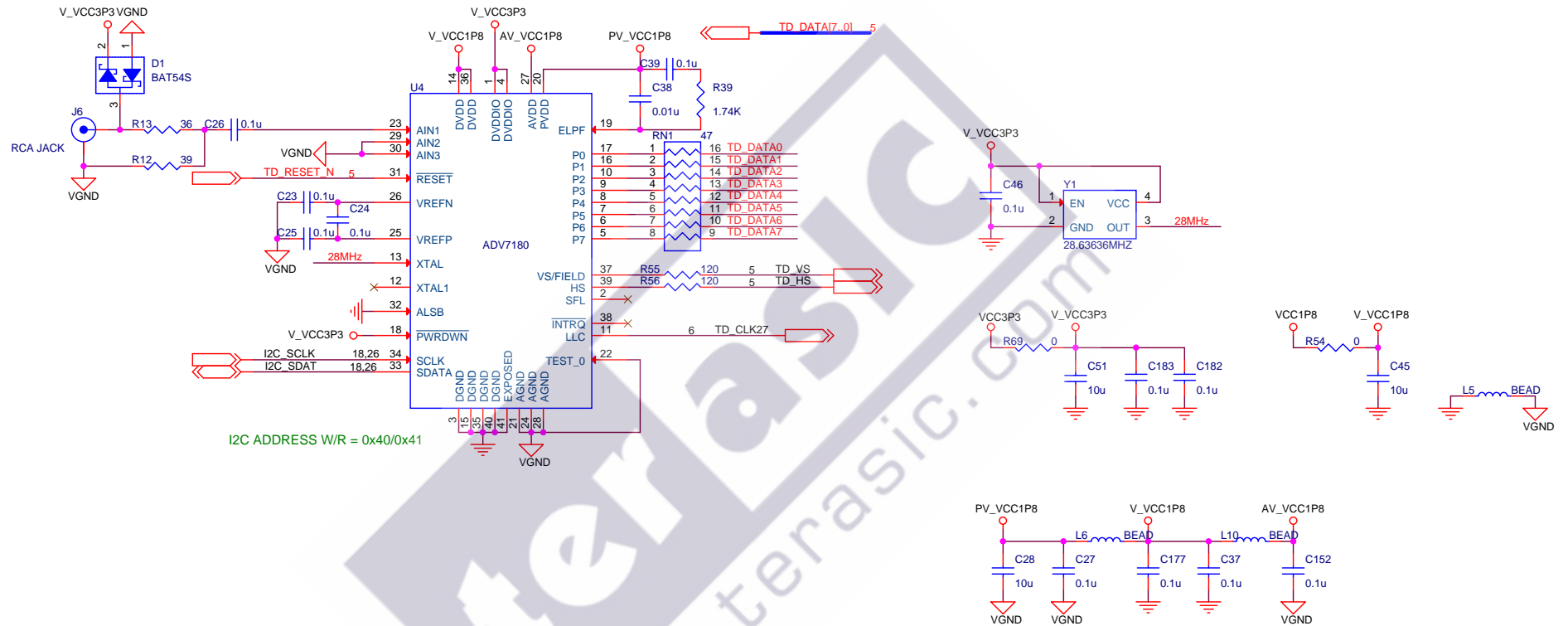


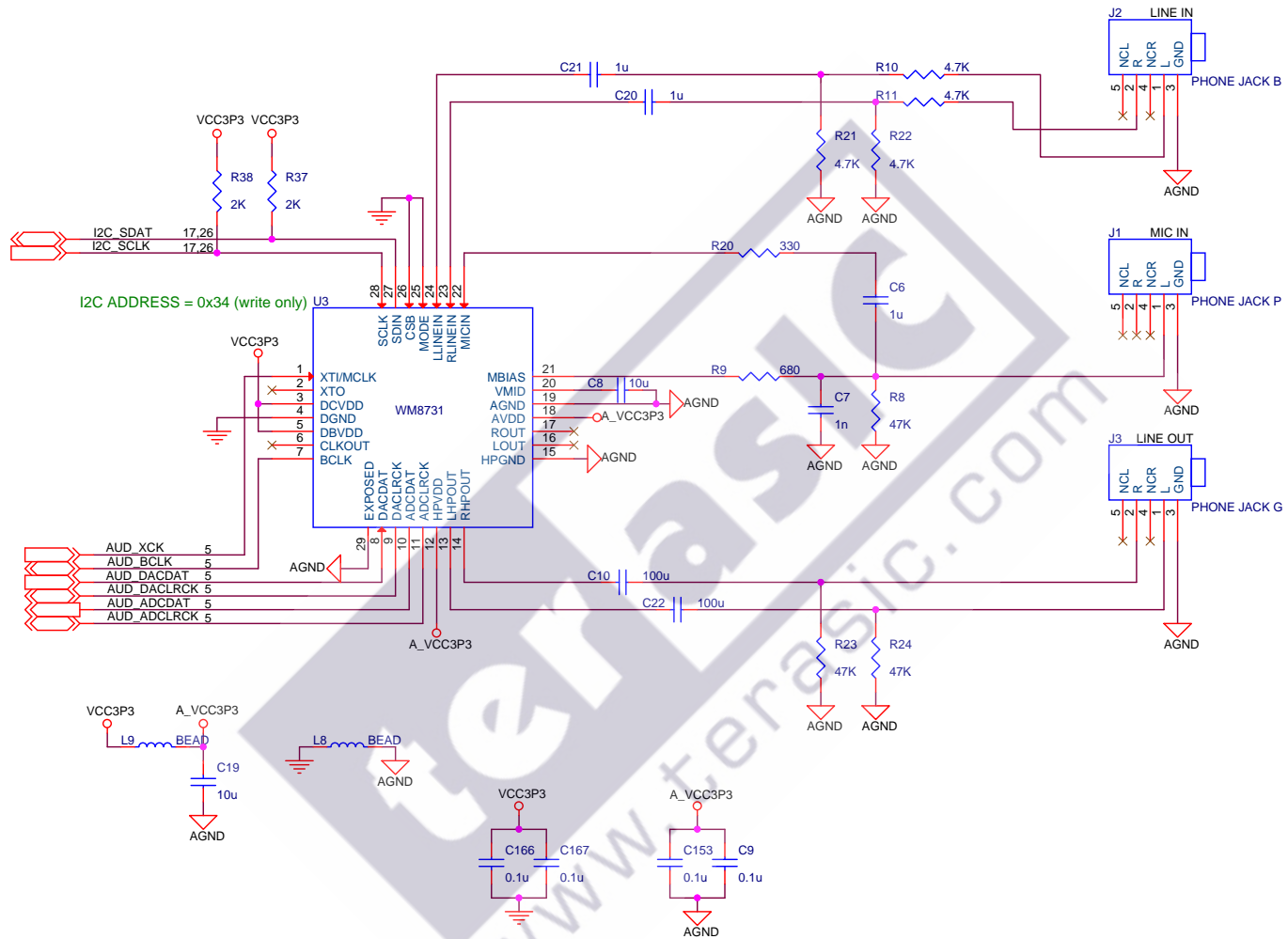
Note: you can only swap the DQ signals within x8 group (e.g. 0-7,8-15,16-23,24-31) on the DDR3 chips Note: you can swap the signals on the OCT resistor array(include NC pin)




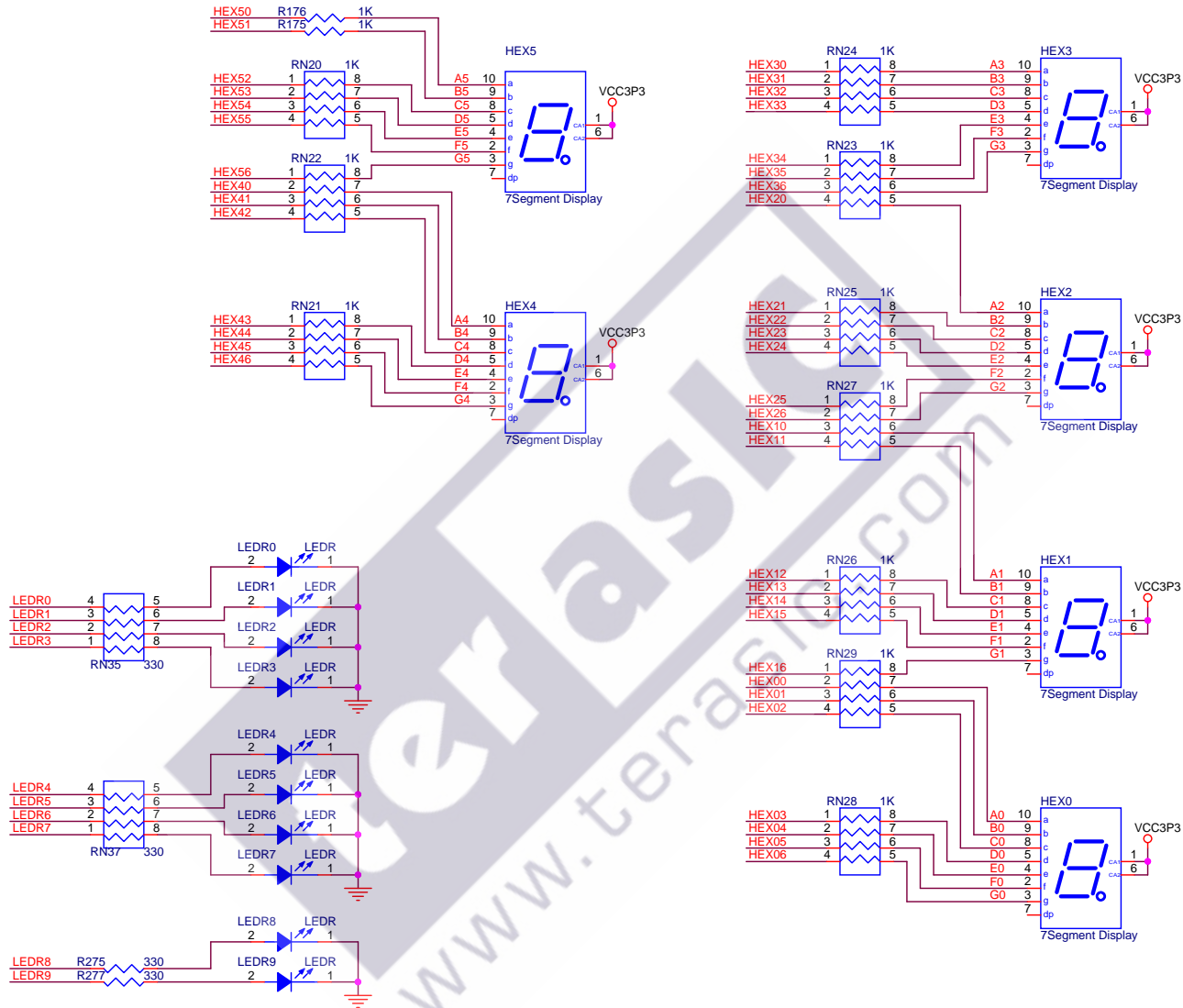
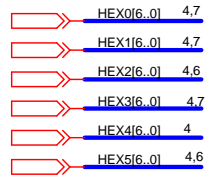
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Title		
DE1-SoC Board		
Size	Document Number	Rev
B	HPS DDR3 SDRAM	F
Date:	Thursday, November 20, 2014	Sheet 15 of 30





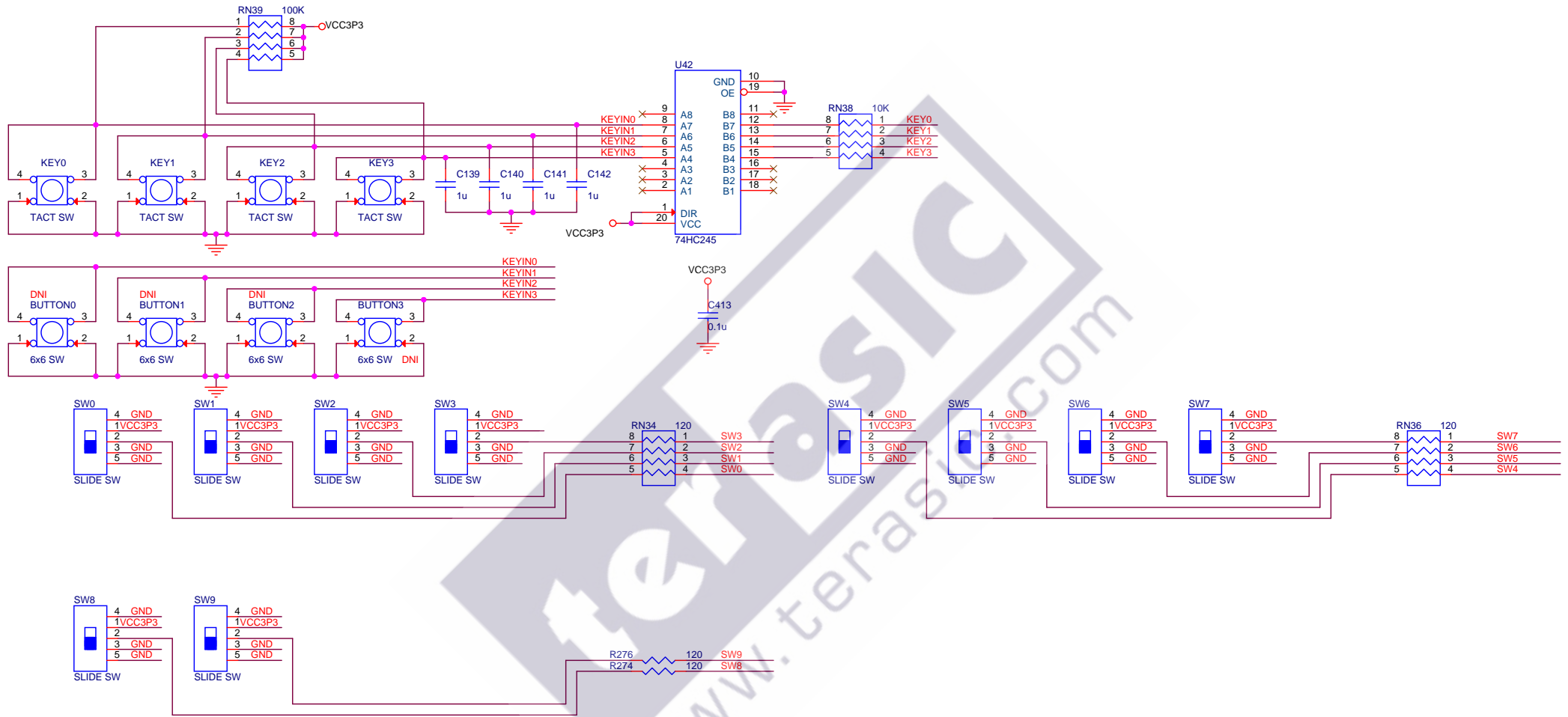


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Title	
DE1-SoC Board	
Size	Document Number
B	Audio CODEC
Date:	Thursday, November 20, 2014
Sheet	18 of 30
Rev	F

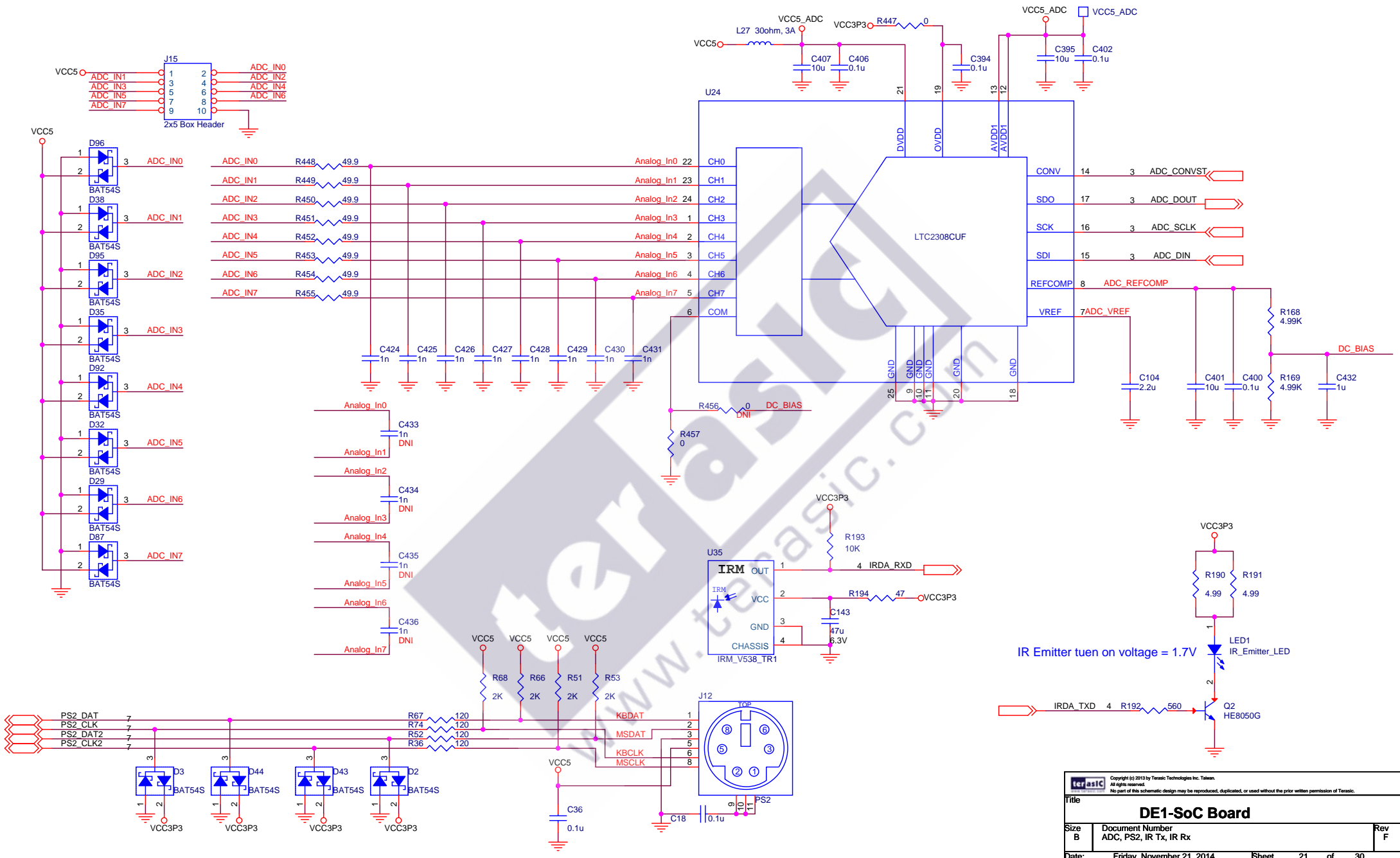


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Title		
DE1-SoC Board		
Size	Document Number	Rev
B	7-Segment Display, LED	F
Date:	Thursday, November 20, 2014	Sheet 19 of 30

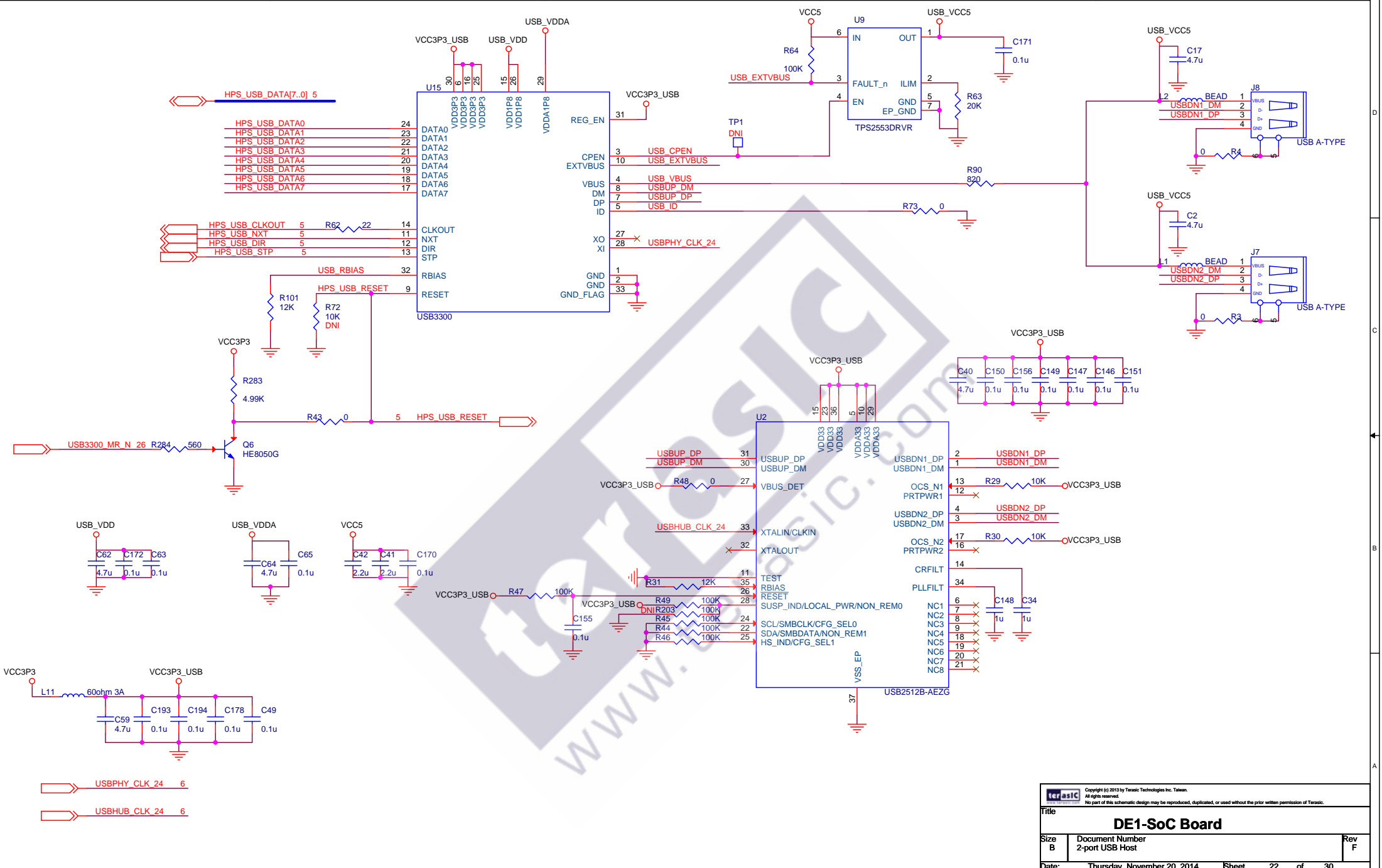
KEY[3..0] 3.6
 SW[9..0] 3.7

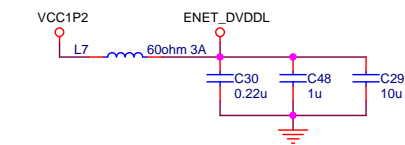
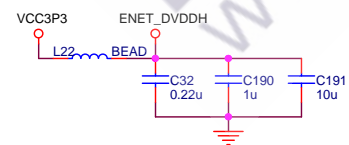
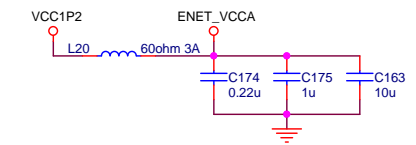
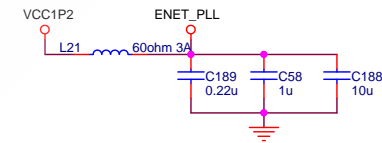
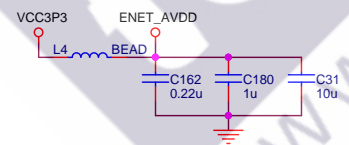
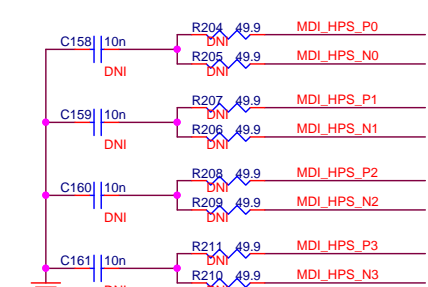
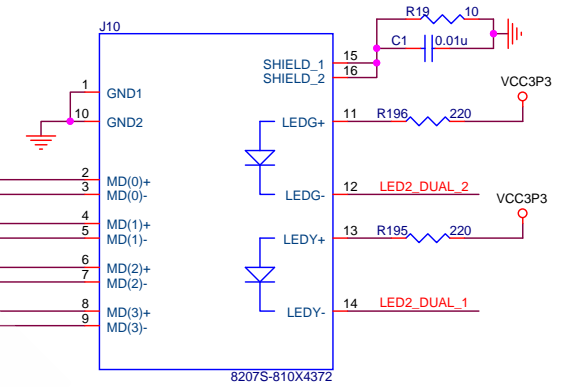
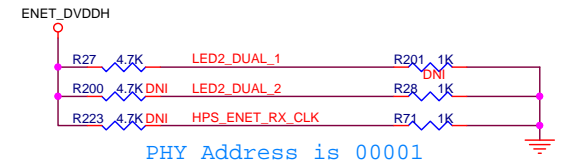
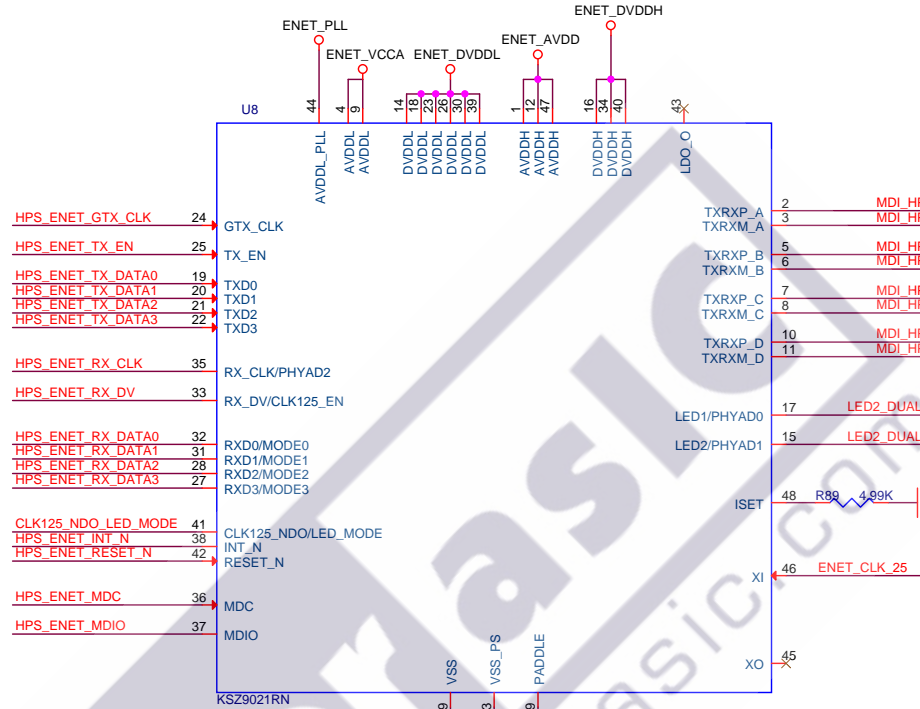
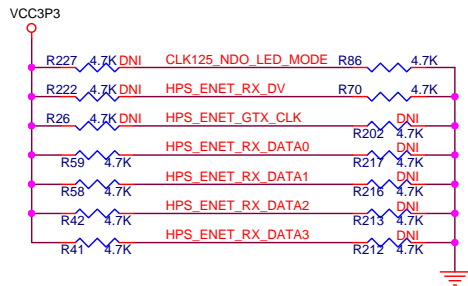
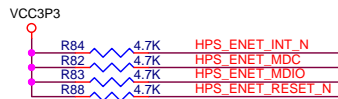
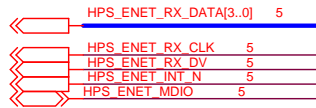
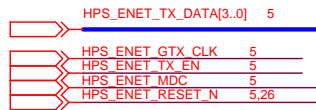


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Title		
DE1-SoC Board		
Size	Document Number	Rev
B	FPGA BUTTON, Switch	F
Date:	Thursday, November 20, 2014	Sheet 20 of 30



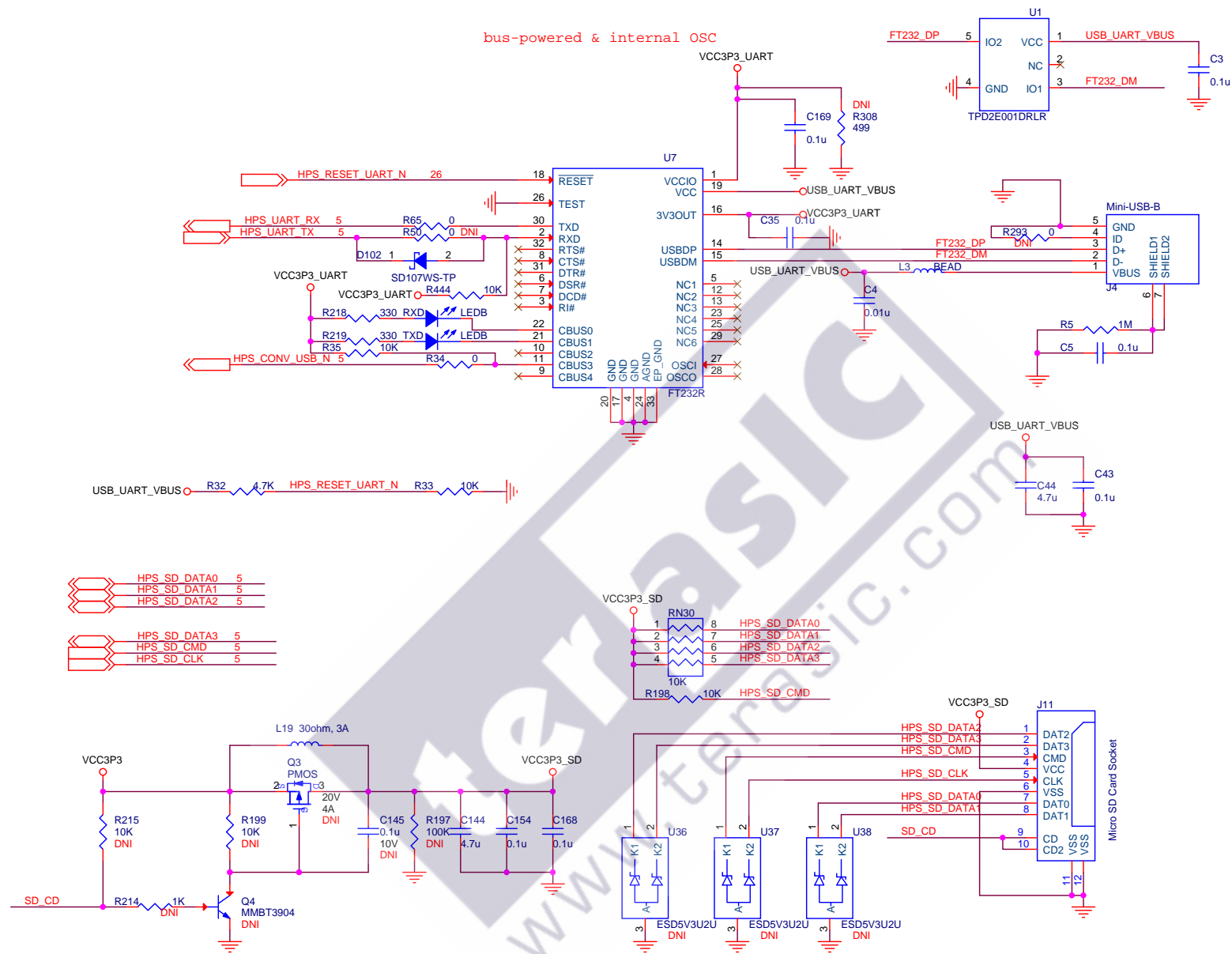
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Title		
DE1-SoC Board		
Size	Document Number	Rev
B	ADC, PS2, IR Tx, IR Rx	F
Date:	Friday, November 21, 2014	Sheet 21 of 30





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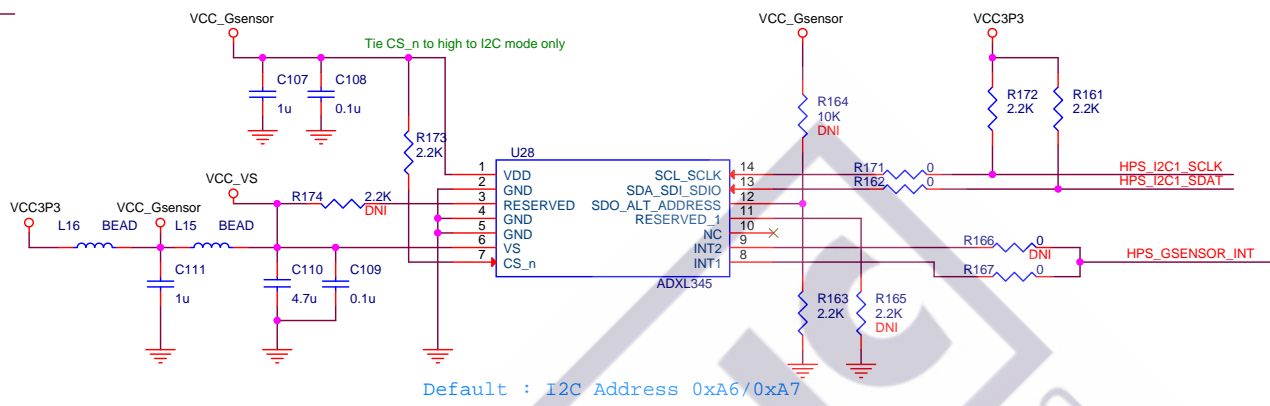
Title		
DE1-SoC Board		
Size	Document Number	Rev
B	1 Gigabit Ethernet	F
Date:	Thursday, March 09, 2017	Sheet 23 of 30



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Title		
DE1-SoC Board		
Size	Document Number	Rev
B	UART to USB, SD CARD	F
Date:	Thursday, November 20, 2014	Sheet 24 of 30

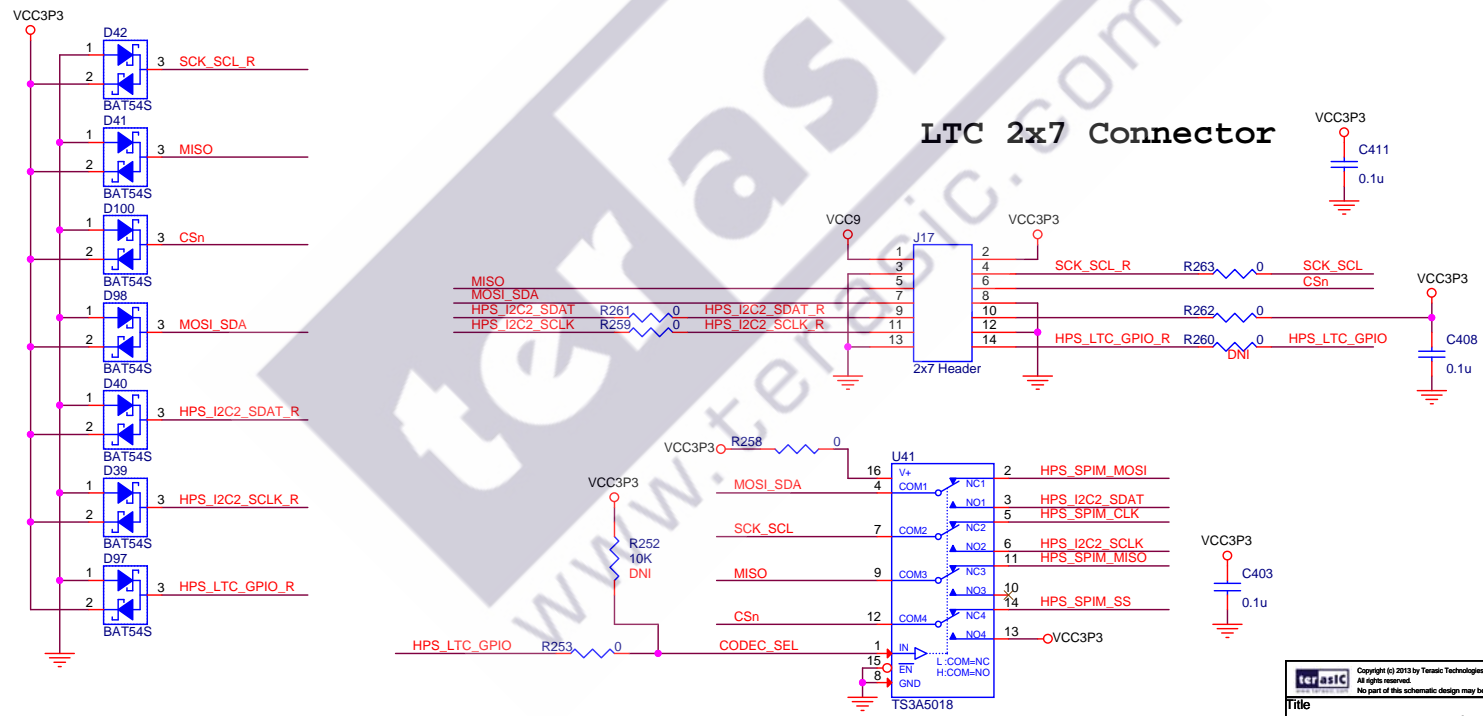
- HPS_I2C1_SDAT 5,26
- HPS_I2C1_SCLK 5,26
- HPS_GSENSOR_INT 5

Digital Accelerometer

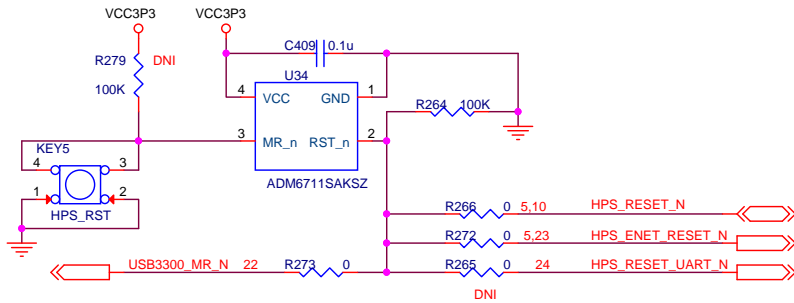


- HPS_I2C2_SCLK 5
- HPS_I2C2_SDAT 5
- HPS_SPIM_MOSI 5
- HPS_SPIM_CLK 5
- HPS_SPIM_SS 5
- HPS_SPIM_MISO 5
- HPS_LTC_GPIO 5

LTC 2x7 Connector

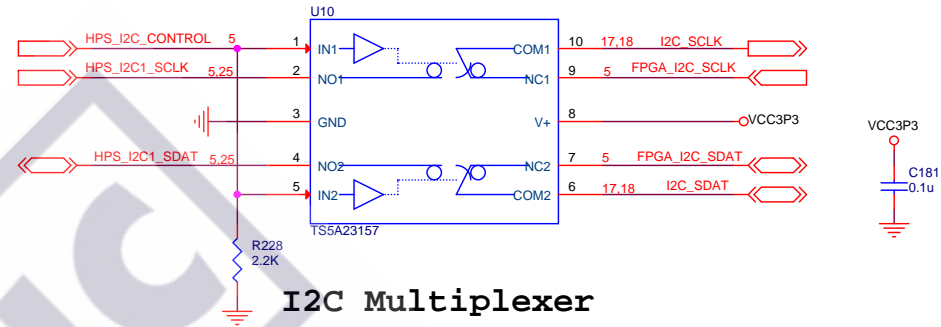


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Title		
DE1-SoC Board		
Size	Document Number	Rev
B	Accelerometer, LTC Connector	F
Date:	Thursday, November 20, 2014	Sheet 25 of 30

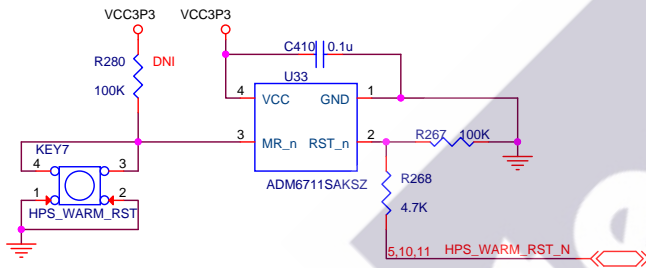


HPS Cold Reset

LOW --> NC to/from COM = ON and NO to/from COM = OFF
 HIGH --> NC to/from COM = OFF and NO to/from COM = ON



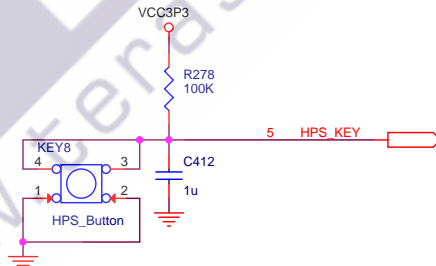
I2C Multiplexer




HPS Warm Reset

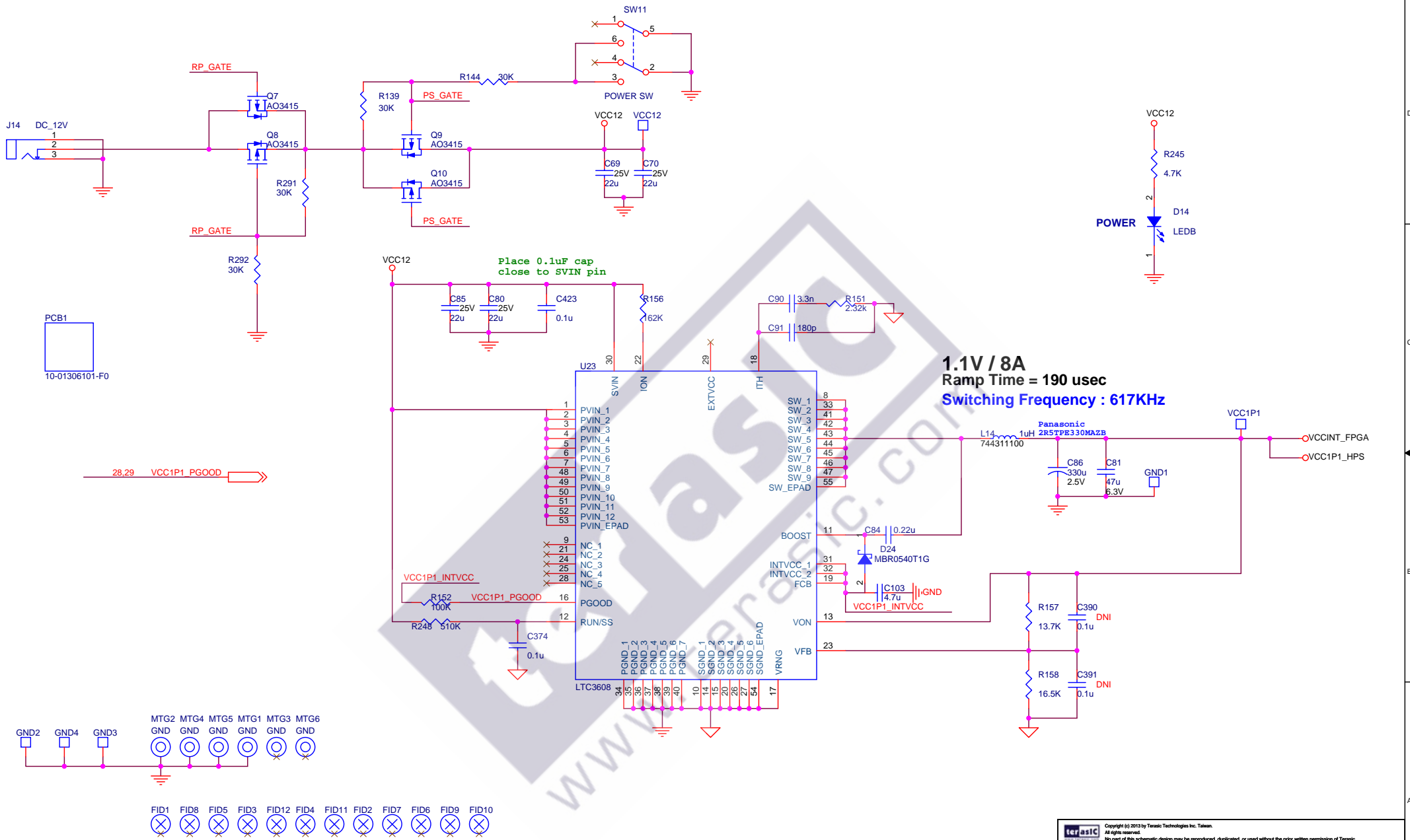


HPS User LED

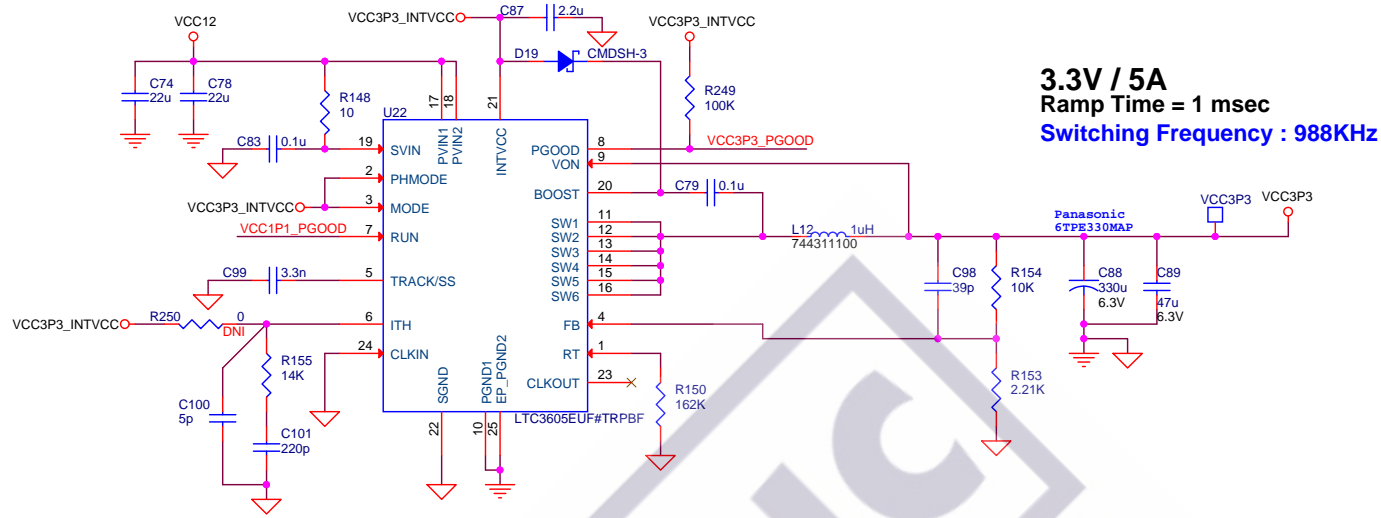


HPS User Button

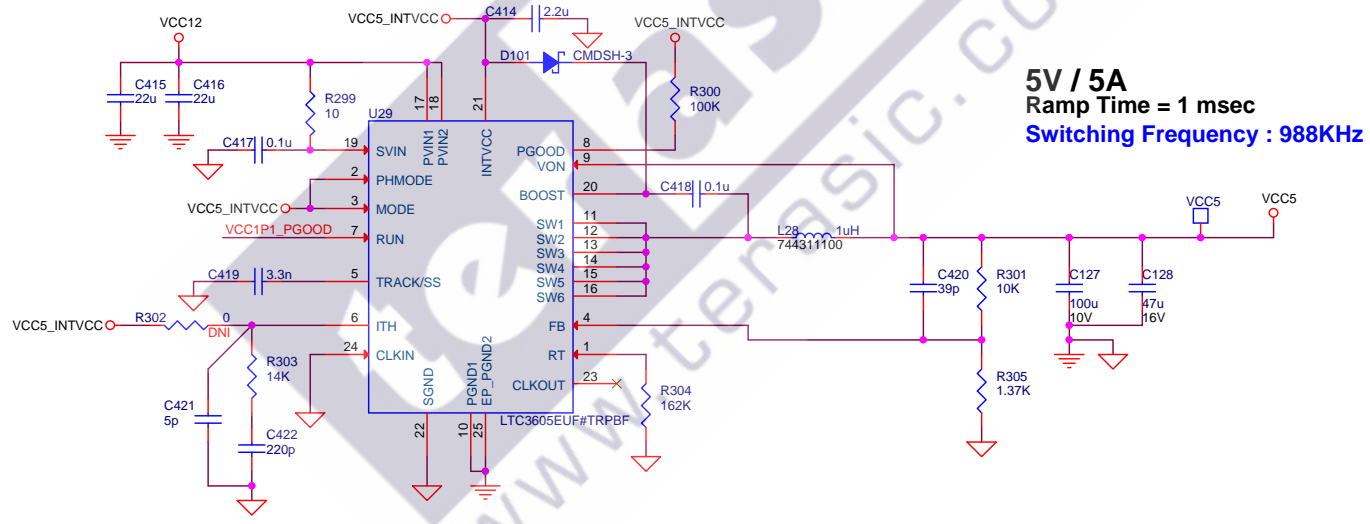
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Title		
DE1-SoC Board		
Size	Document Number	Rev
B	I2C Multiplexer, HPS BUTTON, HPS LED	F
Date:	Thursday, November 20, 2014	Sheet 26 of 30



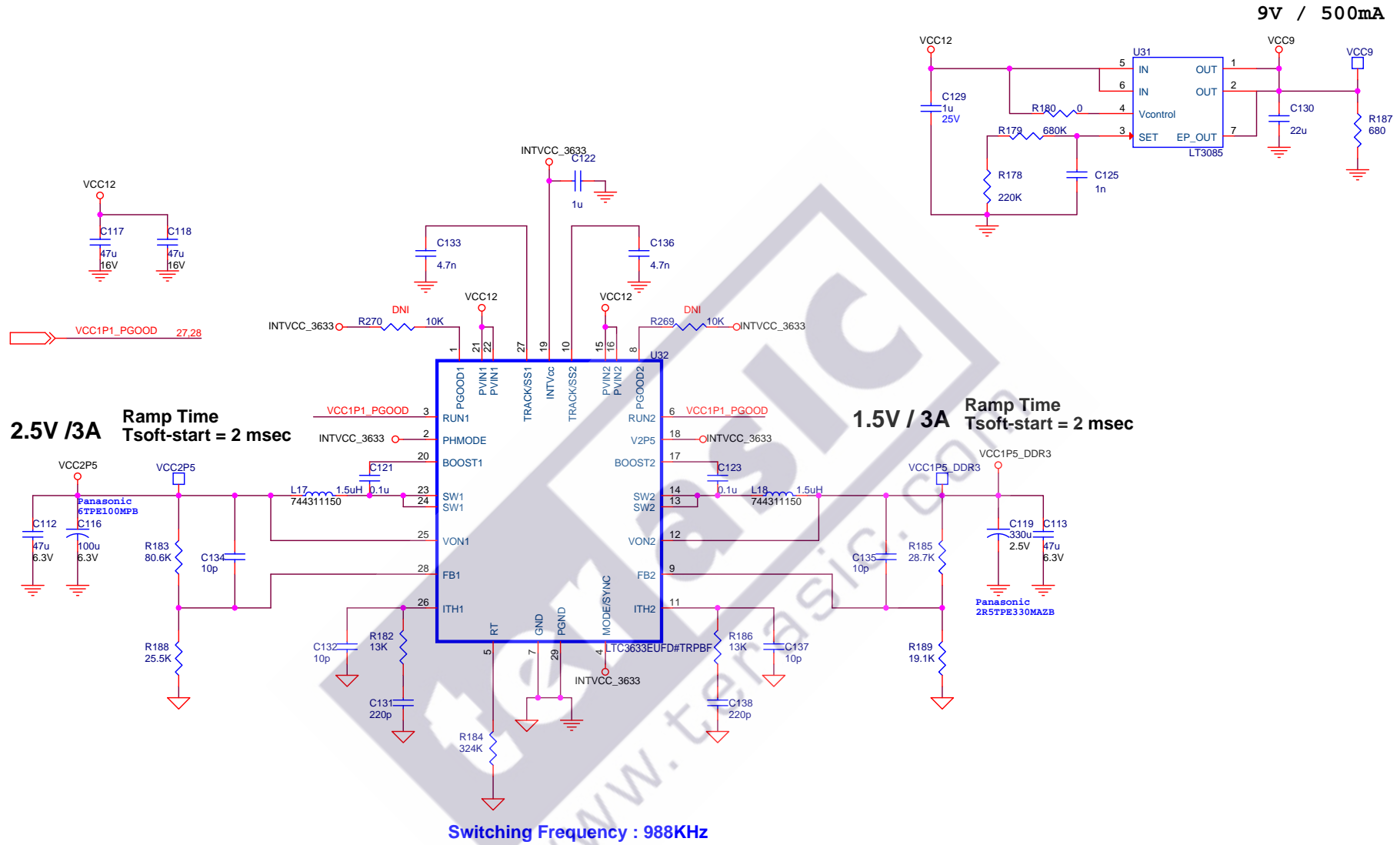
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Title		
DE1-SoC Board		
Size B	Document Number Power - 1.1V	Rev F
Date:	Wednesday, May 27, 2015	Sheet 27 of 30




VCC1P1_PGOOD 27,29

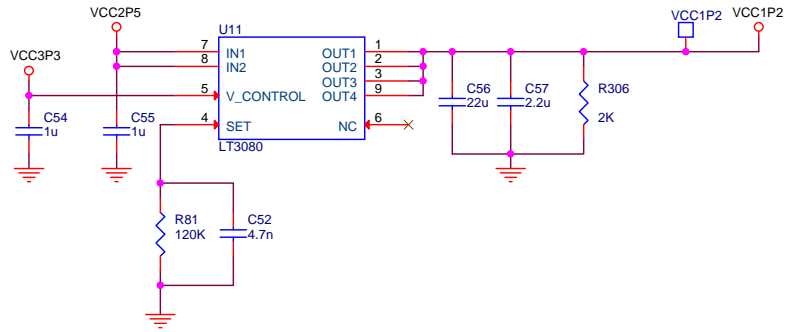


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Title		
DE1-SoC Board		
Size	Document Number	Rev
B	Power - 5V, 3.3V	F
Date:	Wednesday, May 27, 2015	Sheet 28 of 30

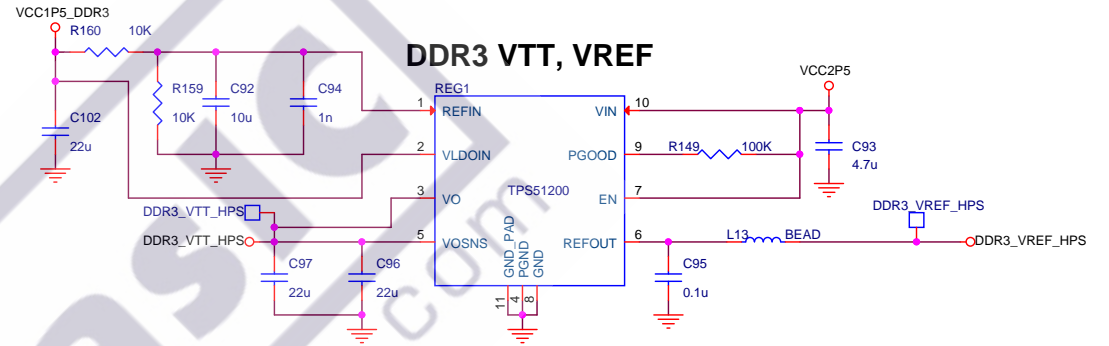


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Title		
DE1-SoC Board		
Size	Document Number	Rev
B	Power - 9V, 2.5V, 1.5V	F
Date:	Wednesday, May 27, 2015	Sheet 29 of 30

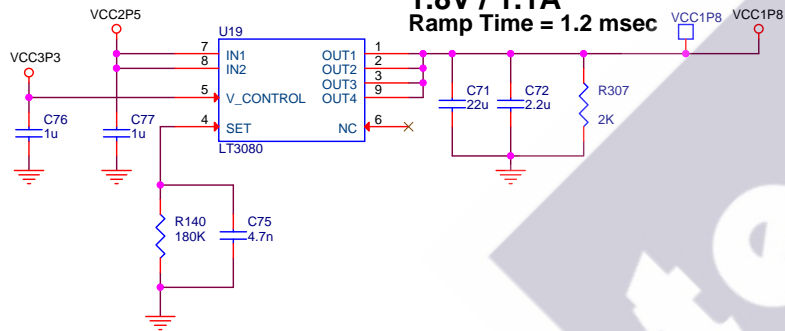
1.2V / 1.1A
Ramp Time = 0.8msec



DDR3 VTT, VREF



1.8V / 1.1A
Ramp Time = 1.2 msec



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Title	
DE1-SoC Board	
Size B	Document Number Power - 1.2V, 1.8V, DDR3 VREF, DDR3 VTT
Date:	Thursday, November 20, 2014
Sheet	30 of 30
Rev	F