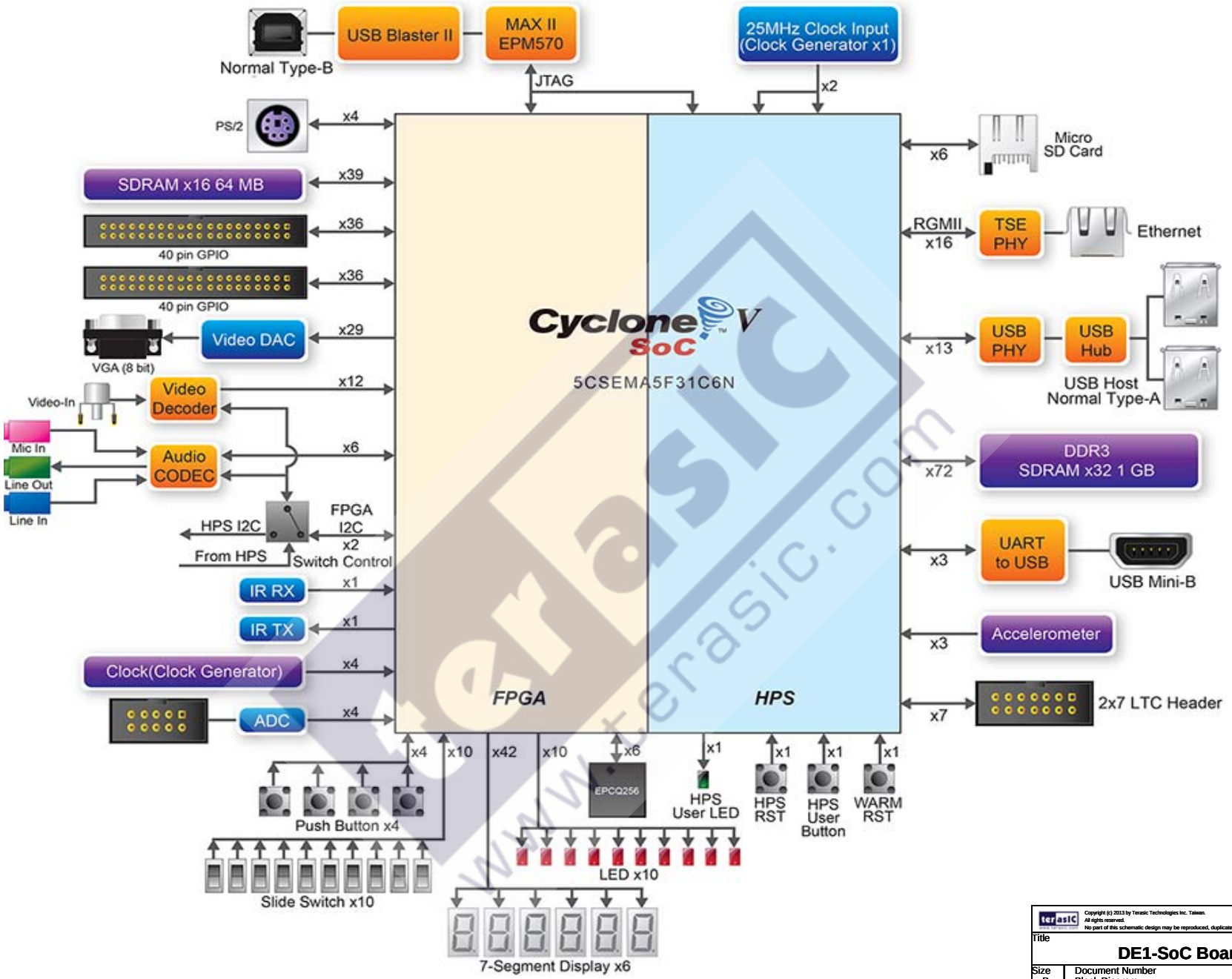
ALTERA Cyclone V SoC Development & Education Board (DE1-SoC)

Title: **DE1-SoC Board**

Size	Document Number	Rev
B	Cover Page	C

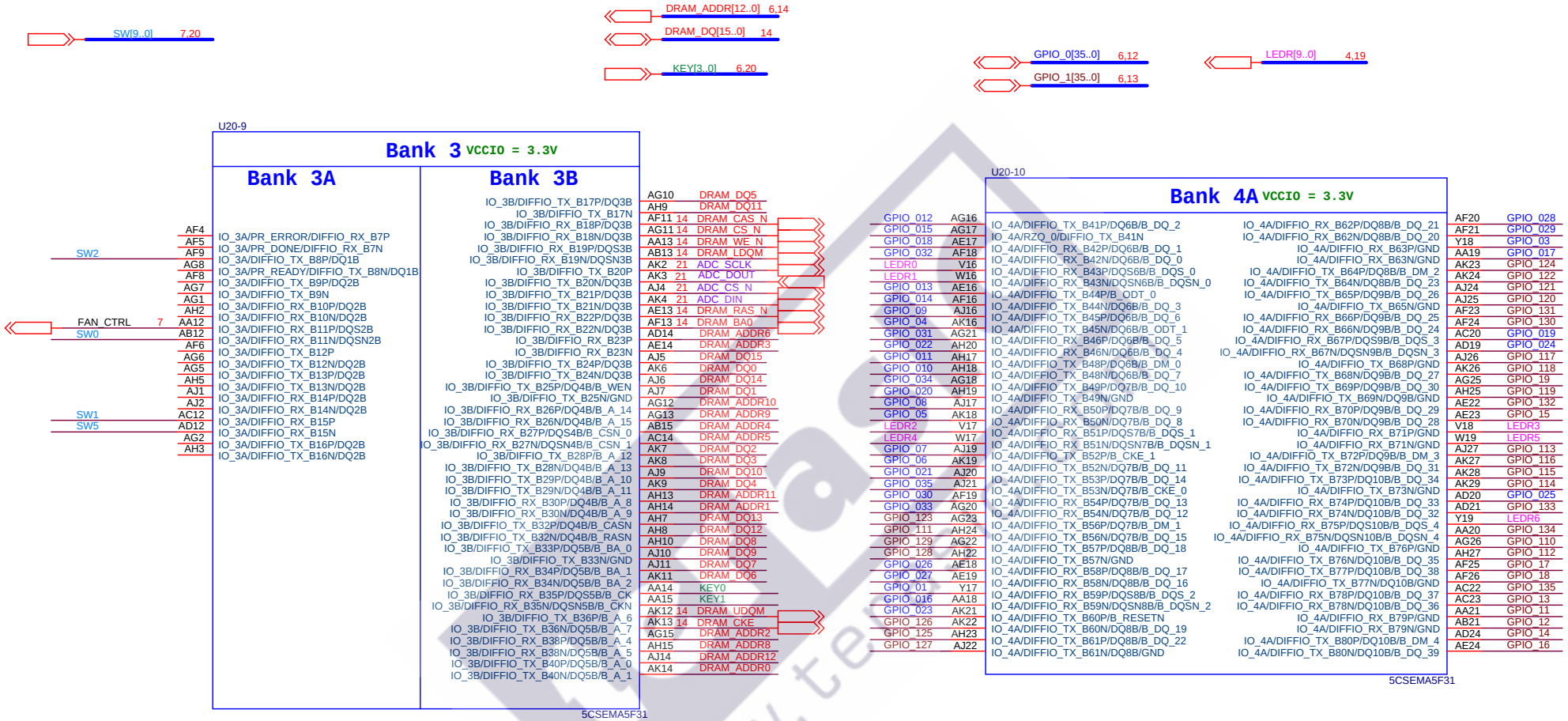
Date: Monday, March 24, 2014 Sheet 1 of 30



Title: **DE1-SoC Board**

Size	Document Number	Rev
B	Block Diagram	C

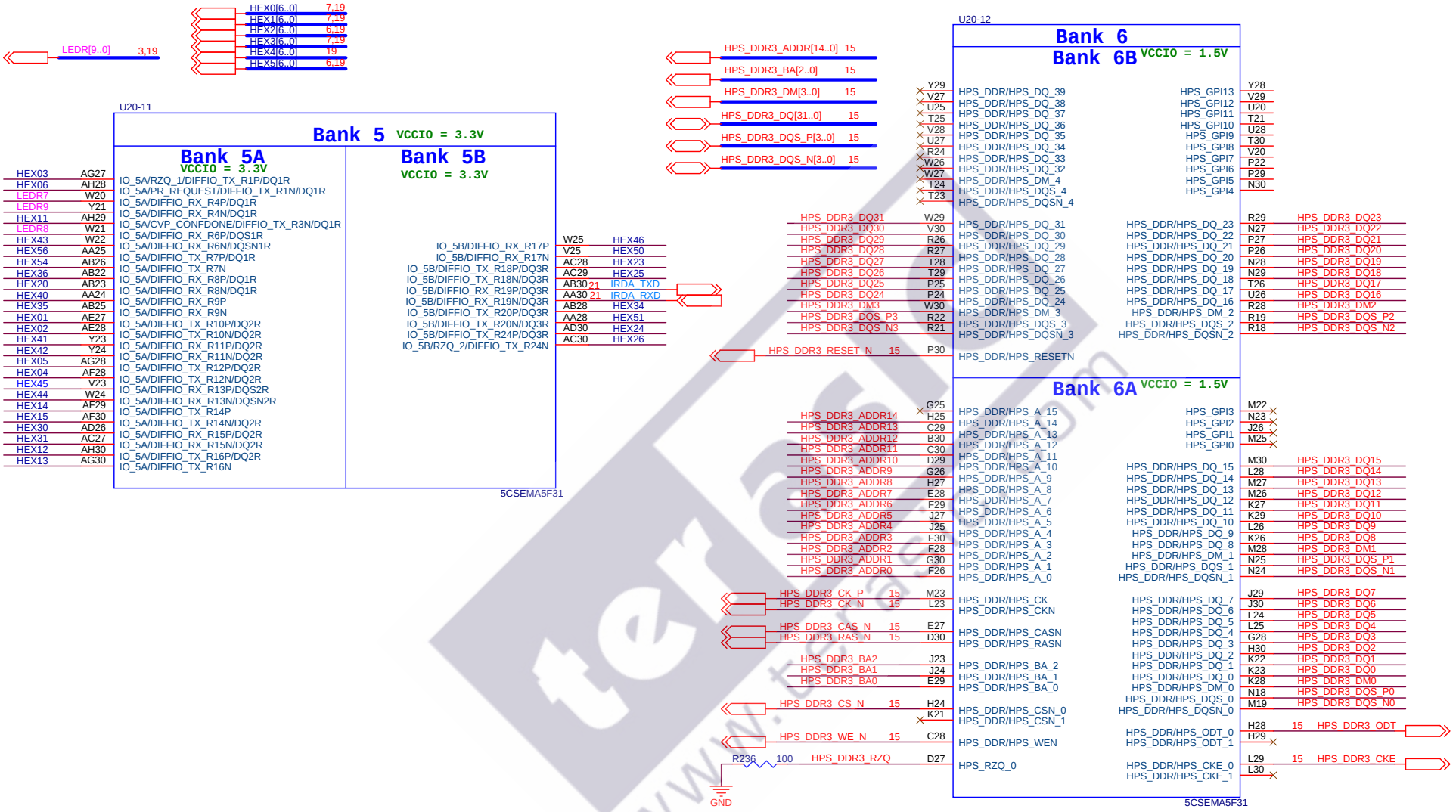
Date: Monday, March 24, 2014 Sheet 2 of 30

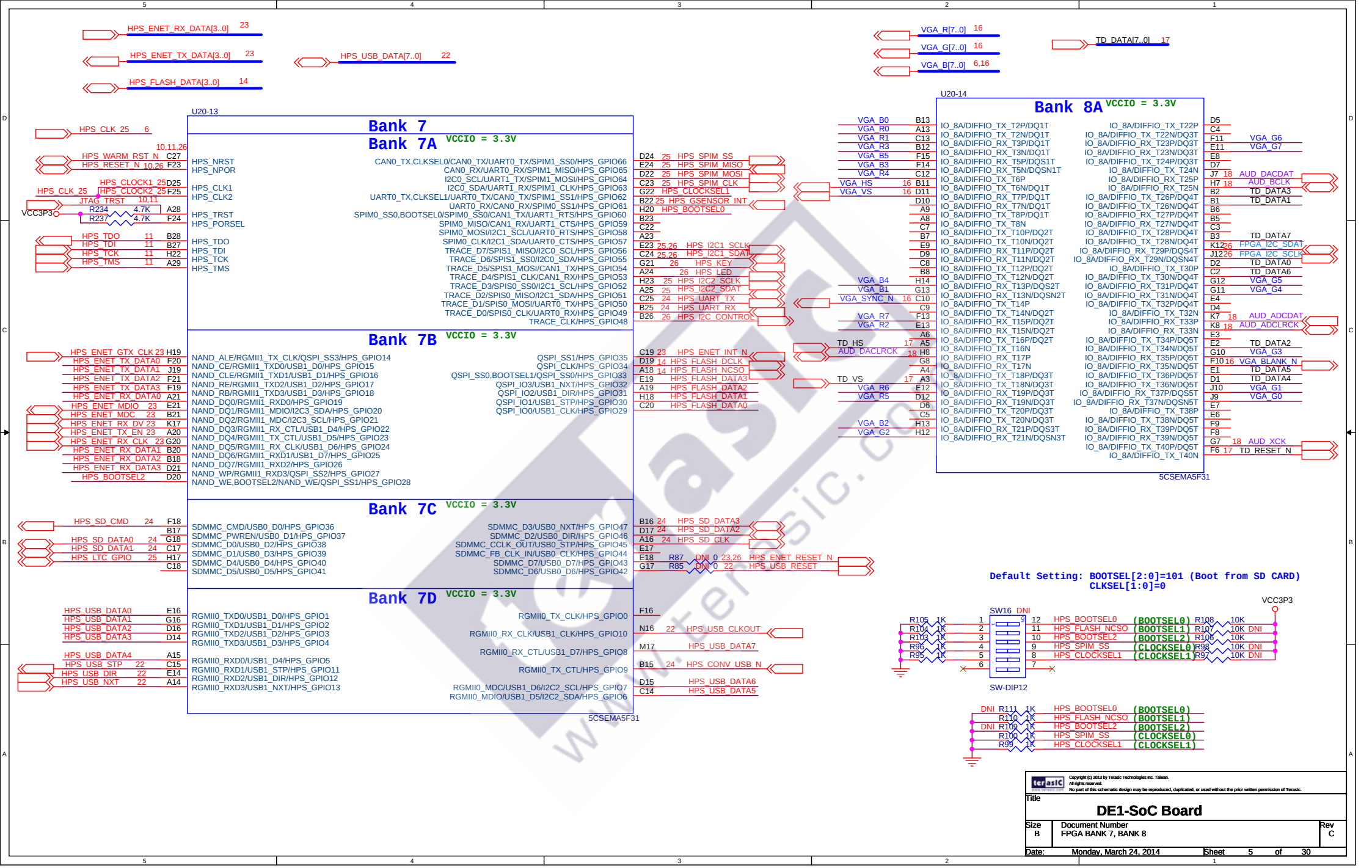


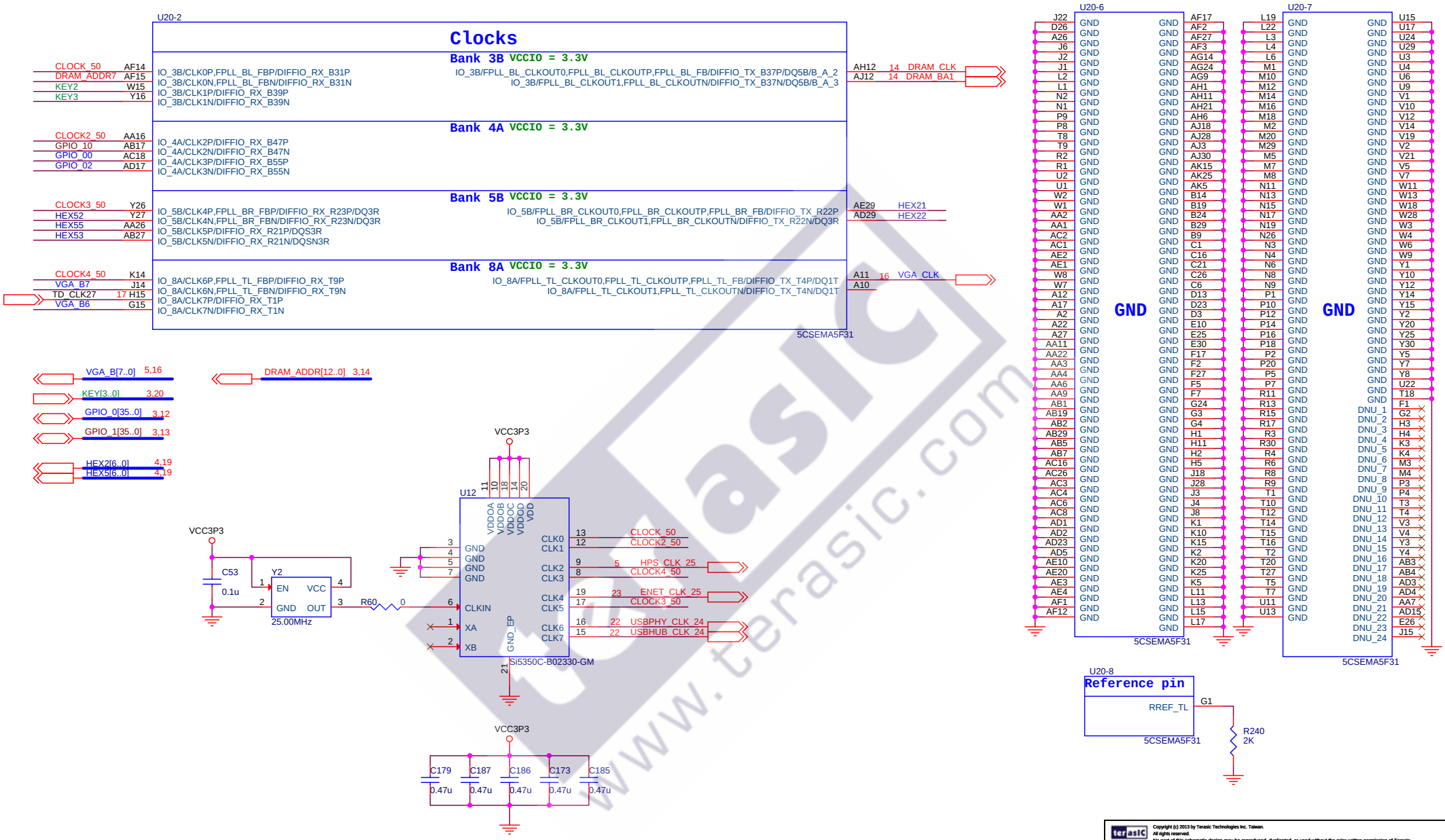
Title: **DE1-SoC Board**

Size	Document Number	Rev
B	FPGA BANK 3, BANK 4	C

Date: Monday, March 24, 2014 Sheet 3 of 30


LEDR[9..0] 3,19
HEX0[6..0] 7,19
HEX1[6..0] 7,19
HEX2[6..0] 6,19
HEX3[6..0] 7,19
HEX4[6..0] 19
HEX5[6..0] 6,19
U20-11
Bank 5 VCCIO = 3.3V
Bank 5A
VCCIO = 3.3V
HEX03 AG27 IO_5A/RZQ_1/DIFFIO_TX_R1P/DQ1R
HEX06 AH28 IO_5A/PR_REQUEST/DIFFIO_TX_R1N/DQ1R
LEDR7 W20 IO_5A/DIFFIO_RX_R4P/DQ1R
LEDR9 Y21 IO_5A/DIFFIO_RX_R4N/DQ1R
HEX11 AH29 IO_5A/CVP_CONFDONE/DIFFIO_TX_R3N/DQ1R
LEDR8 W21 IO_5A/DIFFIO_RX_R6P/DQS1R
HEX43 W22 IO_5A/DIFFIO_RX_R6N/DQSN1R
HEX56 AA25 IO_5A/DIFFIO_TX_R7P/DQ1R
HEX54 AB26 IO_5A/DIFFIO_TX_R7N
HEX36 AB22 IO_5A/DIFFIO_RX_R8P/DQ1R
HEX20 AB23 IO_5A/DIFFIO_RX_R8N/DQ1R
HEX40 AA24 IO_5A/DIFFIO_RX_R9P
HEX35 AB25 IO_5A/DIFFIO_RX_R9N
HEX01 AE27 IO_5A/DIFFIO_TX_R10P/DQ2R
HEX02 AE28 IO_5A/DIFFIO_TX_R10N/DQ2R
HEX41 Y23 IO_5A/DIFFIO_RX_R11P/DQ2R
HEX42 Y24 IO_5A/DIFFIO_RX_R11N/DQ2R
HEX05 AG28 IO_5A/DIFFIO_TX_R12P/DQ2R
HEX04 AF28 IO_5A/DIFFIO_TX_R12N/DQ2R
HEX45 V23 IO_5A/DIFFIO_RX_R13P/DQS2R
HEX44 W24 IO_5A/DIFFIO_RX_R13N/DQSN2R
HEX14 AF29 IO_5A/DIFFIO_TX_R14P
HEX15 AF30 IO_5A/DIFFIO_TX_R14N/DQ2R
HEX30 AD26 IO_5A/DIFFIO_RX_R15P/DQ2R
HEX31 AC27 IO_5A/DIFFIO_RX_R15N/DQ2R
HEX12 AH30 IO_5A/DIFFIO_TX_R16P/DQ2R
HEX13 AG30 IO_5A/DIFFIO_TX_R16N
Bank 5B
VCCIO = 3.3V
IO_5B/DIFFIO_RX_R17P W25 HEX46
IO_5B/DIFFIO_RX_R17N V25 HEX50
IO_5B/DIFFIO_TX_R18P/DQ3R AC28 HEX23
IO_5B/DIFFIO_TX_R18N/DQ3R AC29 HEX25
IO_5B/DIFFIO_RX_R19P/DQ3R AB30 21 IRDA_TXD
IO_5B/DIFFIO_RX_R19N/DQ3R AA30 21 IRDA_RXD
IO_5B/DIFFIO_TX_R20P/DQ3R AB28 HEX34
IO_5B/DIFFIO_TX_R20N/DQ3R AA28 HEX51
IO_5B/DIFFIO_TX_R24P/DQ3R AD30 HEX24
IO_5B/RZQ_2/DIFFIO_TX_R24N AC30 HEX26
5CSEMA5F31
HPS_DDR3_ADDR[14..0] 15
HPS_DDR3_BA[2..0] 15
HPS_DDR3_DM[3..0] 15
HPS_DDR3_DQ[31..0] 15
HPS_DDR3_DQS_P[3..0] 15
HPS_DDR3_DQS_N[3..0] 15
U20-12
Bank 6
Bank 6B VCCIO = 1.5V
Y29 HPS_DDR/HPS_DQ_39
V27 HPS_DDR/HPS_DQ_38
U25 HPS_DDR/HPS_DQ_37
T25 HPS_DDR/HPS_DQ_36
V28 HPS_DDR/HPS_DQ_35
U27 HPS_DDR/HPS_DQ_34
R24 HPS_DDR/HPS_DQ_33
W26 HPS_DDR/HPS_DQ_32
W27 HPS_DDR/HPS_DM_4
T24 HPS_DDR/HPS_DQS_4
T23 HPS_DDR/HPS_DQSN_4
HPS_GPI13 Y28
HPS_GPI12 V29
HPS_GPI11 U20
HPS_GPI10 T21
HPS_GPI9 U28
HPS_GPI8 T30
HPS_GPI7 V20
HPS_GPI6 P22
HPS_GPI5 P29
HPS_GPI4 N30
HPS_DDR3_DQ31 W29 HPS_DDR/HPS_DQ_31 HPS_DDR/HPS_DQ_23 R29 HPS_DDR3_DQ23
HPS_DDR3_DQ30 V30 HPS_DDR/HPS_DQ_30 HPS_DDR/HPS_DQ_22 N27 HPS_DDR3_DQ22
HPS_DDR3_DQ29 R26 HPS_DDR/HPS_DQ_29 HPS_DDR/HPS_DQ_21 P27 HPS_DDR3_DQ21
HPS_DDR3_DQ28 R27 HPS_DDR/HPS_DQ_28 HPS_DDR/HPS_DQ_20 P26 HPS_DDR3_DQ20
HPS_DDR3_DQ27 T28 HPS_DDR/HPS_DQ_27 HPS_DDR/HPS_DQ_19 N28 HPS_DDR3_DQ19
HPS_DDR3_DQ26 T29 HPS_DDR/HPS_DQ_26 HPS_DDR/HPS_DQ_18 N29 HPS_DDR3_DQ18
HPS_DDR3_DQ25 P25 HPS_DDR/HPS_DQ_25 HPS_DDR/HPS_DQ_17 T26 HPS_DDR3_DQ17
HPS_DDR3_DQ24 P24 HPS_DDR/HPS_DQ_24 HPS_DDR/HPS_DQ_16 U26 HPS_DDR3_DQ16
HPS_DDR3_DM3 W30 HPS_DDR/HPS_DM_3 HPS_DDR/HPS_DM_2 R28 HPS_DDR3_DM2
HPS_DDR3_DQS_P3 R22 HPS_DDR/HPS_DQS_3 HPS_DDR/HPS_DQS_2 R19 HPS_DDR3_DQS_P2
HPS_DDR3_DQS_N3 R21 HPS_DDR/HPS_DQSN_3 HPS_DDR/HPS_DQSN_2 R18 HPS_DDR3_DQS_N2
HPS_DDR3_RESET_N 15 P30 HPS_DDR/HPS_RESETN
Bank 6A VCCIO = 1.5V
G25 HPS_DDR/HPS_A_15
HPS_DDR3_ADDR14 H25 HPS_DDR/HPS_A_14
HPS_DDR3_ADDR13 C29 HPS_DDR/HPS_A_13
HPS_DDR3_ADDR12 B30 HPS_DDR/HPS_A_12
HPS_DDR3_ADDR11 C30 HPS_DDR/HPS_A_11
HPS_DDR3_ADDR10 D29 HPS_DDR/HPS_A_10
HPS_DDR3_ADDR9 G26 HPS_DDR/HPS_A_9
HPS_DDR3_ADDR8 H27 HPS_DDR/HPS_A_8
HPS_DDR3_ADDR7 E28 HPS_DDR/HPS_A_7
HPS_DDR3_ADDR6 F29 HPS_DDR/HPS_A_6
HPS_DDR3_ADDR5 J27 HPS_DDR/HPS_A_5
HPS_DDR3_ADDR4 J25 HPS_DDR/HPS_A_4
HPS_DDR3_ADDR3 F30 HPS_DDR/HPS_A_3
HPS_DDR3_ADDR2 F28 HPS_DDR/HPS_A_2
HPS_DDR3_ADDR1 G30 HPS_DDR/HPS_A_1
HPS_DDR3_ADDR0 F26 HPS_DDR/HPS_A_0
HPS_GPI3 M22
HPS_GPI2 N23
HPS_GPI1 J26
HPS_GPI0 M25
M30 HPS_DDR/HPS_DQ_15 M30 HPS_DDR3_DQ15
L28 HPS_DDR/HPS_DQ_14 L28 HPS_DDR3_DQ14
M27 HPS_DDR/HPS_DQ_13 M27 HPS_DDR3_DQ13
M26 HPS_DDR/HPS_DQ_12 M26 HPS_DDR3_DQ12
K27 HPS_DDR/HPS_DQ_11 K27 HPS_DDR3_DQ11
K29 HPS_DDR/HPS_DQ_10 K29 HPS_DDR3_DQ10
L26 HPS_DDR/HPS_DQ_9 L26 HPS_DDR3_DQ9
K26 HPS_DDR/HPS_DQ_8 K26 HPS_DDR3_DQ8
M28 HPS_DDR/HPS_DM_1 M28 HPS_DDR3_DM1
N25 HPS_DDR/HPS_DQS_1 N25 HPS_DDR3_DQS_P1
N24 HPS_DDR/HPS_DQSN_1 N24 HPS_DDR3_DQS_N1
HPS_DDR3_CK_P 15 M23 HPS_DDR/HPS_CK HPS_DDR/HPS_DQ_7 J29 HPS_DDR3_DQ7
HPS_DDR3_CK_N 15 L23 HPS_DDR/HPS_CKN HPS_DDR/HPS_DQ_6 J30 HPS_DDR3_DQ6
HPS_DDR/HPS_DQ_5 L24 HPS_DDR3_DQ5
HPS_DDR3_CAS_N 15 E27 HPS_DDR/HPS_CASN HPS_DDR/HPS_DQ_4 L25 HPS_DDR3_DQ4
HPS_DDR3_RAS_N 15 D30 HPS_DDR/HPS_RASN HPS_DDR/HPS_DQ_3 G28 HPS_DDR3_DQ3
HPS_DDR/HPS_DQ_2 H30 HPS_DDR3_DQ2
HPS_DDR3_BA2 J23 HPS_DDR/HPS_BA_2 HPS_DDR/HPS_DQ_1 K22 HPS_DDR3_DQ1
HPS_DDR3_BA1 J24 HPS_DDR/HPS_BA_1 HPS_DDR/HPS_DQ_0 K23 HPS_DDR3_DQ0
HPS_DDR3_BA0 E29 HPS_DDR/HPS_BA_0 HPS_DDR/HPS_DM_0 K28 HPS_DDR3_DM0
HPS_DDR/HPS_DQS_0 N18 HPS_DDR3_DQS_P0
HPS_DDR3_CS_N 15 H24 HPS_DDR/HPS_CSN_0 HPS_DDR/HPS_DQSN_0 M19 HPS_DDR3_DQS_N0
K21 HPS_DDR/HPS_CSN_1
HPS_DDR/HPS_ODT_0 H28 15 HPS_DDR3_ODT
HPS_DDR3_WE_N 15 C28 HPS_DDR/HPS_WEN HPS_DDR/HPS_ODT_1 H29
R236 100 HPS_DDR3_RZQ D27 HPS_RZQ_0 HPS_DDR/HPS_CKE_0 L29 15 HPS_DDR3_CKE
HPS_DDR/HPS_CKE_1 L30
GND
5CSEMA5F31
Copyright (c) 2013 by Terasic Technologies Inc. Taiwan.
All rights reserved.
No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.
Title
DE1-SoC Board
Size B
Document Number
FPGA BANK 5, BANK 6
Rev C
Date: Monday, March 24, 2014
Sheet 4 of 30


HPS_ENET_RX_DATA[3..0] 23
HPS_ENET_TX_DATA[3..0] 23
HPS_FLASH_DATA[3..0] 14
HPS_USB_DATA[7..0] 22
VGA_R[7..0] 16
VGA_G[7..0] 16
VGA_B[7..0] 6,16
TD_DATA[7..0] 17
U20-13
Bank 7
Bank 7A
VCCIO = 3.3V
HPS_CLK_25 6
HPS_WARM_RST_N C27
HPS_RESET_N 10,26 F23
HPS_CLOCK1_25 D25
HPS_CLOCK2_25 F25
JTAG_TRST 10,11
VCC3P3
R234 4.7K A28
R237 4.7K F24
HPS_TDO 11 B28
HPS_TDI 11 B27
HPS_TCK 11 H22
HPS_TMS 11 A29
HPS_NRST
HPS_NPOR
HPS_CLK1
HPS_CLK2
HPS_TRST
HPS_PORSEL
HPS_TDO
HPS_TDI
HPS_TCK
HPS_TMS
CAN0_TX,CLKSEL0/CAN0_TX/UART0_TX/SPIM1_SS0/HPS_GPIO66
CAN0_RX/UART0_RX/SPIM1_MISO/HPS_GPIO65
I2C0_SCL/UART1_TX/SPIM1_MOSI/HPS_GPIO64
I2C0_SDA/UART1_RX/SPIM1_CLK/HPS_GPIO63
UART0_TX,CLKSEL1/UART0_TX/CAN0_TX/SPIM1_SS1/HPS_GPIO62
UART0_RX/CAN0_RX/SPIM0_SS1/HPS_GPIO61
SPIM0_SS0,BOOTSEL0/SPIM0_SS0/CAN1_TX/UART1_RTS/HPS_GPIO60
SPIM0_MISO/CAN1_RX/UART1_CTS/HPS_GPIO59
SPIM0_MOSI/I2C1_SCL/UART0_RTS/HPS_GPIO58
SPIM0_CLK/I2C1_SDA/UART0_CTS/HPS_GPIO57
TRACE_D7/SPIS1_MISO/I2C0_SCL/HPS_GPIO56
TRACE_D6/SPIS1_SS0/I2C0_SDA/HPS_GPIO55
TRACE_D5/SPIS1_MOSI/CAN1_TX/HPS_GPIO54
TRACE_D4/SPIS1_CLK/CAN1_RX/HPS_GPIO53
TRACE_D3/SPIS0_SS0/I2C1_SCL/HPS_GPIO52
TRACE_D2/SPIS0_MISO/I2C1_SDA/HPS_GPIO51
TRACE_D1/SPIS0_MOSI/UART0_TX/HPS_GPIO50
TRACE_D0/SPIS0_CLK/UART0_RX/HPS_GPIO49
TRACE_CLK/HPS_GPIO48
D24 25 HPS_SPIM_SS
E24 25 HPS_SPIM_MISO
D22 25 HPS_SPIM_MOSI
C23 25 HPS_SPIM_CLK
G22 HPS_CLOCKSEL1
B22 25 HPS_GSENSOR_INT
H20 HPS_BOOTSEL0
B23
C22
A23
E23 25,26 HPS_I2C1_SCLK
C24 25,26 HPS_I2C1_SDAT
G21 26 HPS_KEY
A24 26 HPS_LED
H23 25 HPS_I2C2_SCLK
A25 25 HPS_I2C2_SDAT
C25 24 HPS_UART_TX
B25 24 HPS_UART_RX
B26 26 HPS_I2C_CONTROL
Bank 7B
VCCIO = 3.3V
HPS_ENET_GTX_CLK 23 H19
HPS_ENET_TX_DATA0 F20
HPS_ENET_TX_DATA1 J19
HPS_ENET_TX_DATA2 F21
HPS_ENET_TX_DATA3 F19
HPS_ENET_RX_DATA0 A21
HPS_ENET_MDIO 23 E21
HPS_ENET_MDC 23 B21
HPS_ENET_RX_DV 23 K17
HPS_ENET_TX_EN 23 A20
HPS_ENET_RX_CLK 23 G20
HPS_ENET_RX_DATA1 B20
HPS_ENET_RX_DATA2 B18
HPS_ENET_RX_DATA3 D21
HPS_BOOTSEL2 D20
NAND_ALE/RGMII1_TX_CLK/QSPI_SS3/HPS_GPIO14
NAND_CE/RGMII1_TXD0/USB1_D0/HPS_GPIO15
NAND_CLE/RGMII1_TXD1/USB1_D1/HPS_GPIO16
NAND_RE/RGMII1_TXD2/USB1_D2/HPS_GPIO17
NAND_RB/RGMII1_TXD3/USB1_D3/HPS_GPIO18
NAND_DQ0/RGMII1_RXD0/HPS_GPIO19
NAND_DQ1/RGMII1_MDIO/I2C3_SDA/HPS_GPIO20
NAND_DQ2/RGMII1_MDC/I2C3_SCL/HPS_GPIO21
NAND_DQ3/RGMII1_RX_CTL/USB1_D4/HPS_GPIO22
NAND_DQ4/RGMII1_TX_CTL/USB1_D5/HPS_GPIO23
NAND_DQ5/RGMII1_RX_CLK/USB1_D6/HPS_GPIO24
NAND_DQ6/RGMII1_RXD1/USB1_D7/HPS_GPIO25
NAND_DQ7/RGMII1_RXD2/HPS_GPIO26
NAND_WP/RGMII1_RXD3/QSPI_SS2/HPS_GPIO27
NAND_WE,BOOTSEL2/NAND_WE/QSPI_SS1/HPS_GPIO28
QSPI_SS1/HPS_GPIO35
QSPI_CLK/HPS_GPIO34
QSPI_SS0,BOOTSEL1/QSPI_SS0/HPS_GPIO33
QSPI_IO3/USB1_NXT/HPS_GPIO32
QSPI_IO2/USB1_DIR/HPS_GPIO31
QSPI_IO1/USB1_STP/HPS_GPIO30
QSPI_IO0/USB1_CLK/HPS_GPIO29
C19 23 HPS_ENET_INT_N
D19 14 HPS_FLASH_DCLK
A18 14 HPS_FLASH_NCSO
E19 HPS_FLASH_DATA3
A19 HPS_FLASH_DATA2
H18 HPS_FLASH_DATA1
C20 HPS_FLASH_DATA0
Bank 7C
VCCIO = 3.3V
HPS_SD_CMD 24 F18
B17
HPS_SD_DATA0 24 G18
HPS_SD_DATA1 24 C17
HPS_LTC_GPIO 25 H17
C18
SDMMC_CMD/USB0_D0/HPS_GPIO36
SDMMC_PWREN/USB0_D1/HPS_GPIO37
SDMMC_D0/USB0_D2/HPS_GPIO38
SDMMC_D1/USB0_D3/HPS_GPIO39
SDMMC_D4/USB0_D4/HPS_GPIO40
SDMMC_D5/USB0_D5/HPS_GPIO41
SDMMC_D3/USB0_NXT/HPS_GPIO47
SDMMC_D2/USB0_DIR/HPS_GPIO46
SDMMC_CCLK_OUT/USB0_STP/HPS_GPIO45
SDMMC_FB_CLK_IN/USB0_CLK/HPS_GPIO44
SDMMC_D7/USB0_D7/HPS_GPIO43
SDMMC_D6/USB0_D6/HPS_GPIO42
B16 24 HPS_SD_DATA3
D17 24 HPS_SD_DATA2
A16 24 HPS_SD_CLK
E17
E18 R87 DNI 0 23,26 HPS_ENET_RESET_N
G17 R85 DNI 0 22 HPS_USB_RESET
Bank 7D
VCCIO = 3.3V
HPS_USB_DATA0 E16
HPS_USB_DATA1 G16
HPS_USB_DATA2 D16
HPS_USB_DATA3 D14
HPS_USB_DATA4 A15
HPS_USB_STP 22 C15
HPS_USB_DIR 22 E14
HPS_USB_NXT 22 A14
RGMII0_TXD0/USB1_D0/HPS_GPIO1
RGMII0_TXD1/USB1_D1/HPS_GPIO2
RGMII0_TXD2/USB1_D2/HPS_GPIO3
RGMII0_TXD3/USB1_D3/HPS_GPIO4
RGMII0_RXD0/USB1_D4/HPS_GPIO5
RGMII0_RXD1/USB1_STP/HPS_GPIO11
RGMII0_RXD2/USB1_DIR/HPS_GPIO12
RGMII0_RXD3/USB1_NXT/HPS_GPIO13
RGMII0_TX_CLK/HPS_GPIO0
RGMII0_RX_CLK/USB1_CLK/HPS_GPIO10
RGMII0_RX_CTL/USB1_D7/HPS_GPIO8
RGMII0_TX_CTL/HPS_GPIO9
RGMII0_MDC/USB1_D6/I2C2_SCL/HPS_GPIO7
RGMII0_MDIO/USB1_D5/I2C2_SDA/HPS_GPIO6
F16
N16 22 HPS_USB_CLKOUT
M17 HPS_USB_DATA7
B15 24 HPS_CONV_USB_N
D15 HPS_USB_DATA6
C14 HPS_USB_DATA5
5CSEMA5F31
U20-14
Bank 8A
VCCIO = 3.3V
VGA_B0 B13
VGA_R0 A13
VGA_R1 C13
VGA_R3 B12
VGA_B5 F15
VGA_B3 F14
VGA_R4 C12
VGA_HS 16 B11
VGA_VS 16 D11
VGA_B4 H14
VGA_B1 G13
VGA_SYNC_N 16 C10
C9
VGA_R7 F13
VGA_R2 E13
A6
TD_HS 17 A5
AUD_DACLRCK 18 H8
G8
A4
TD_VS 17 A3
VGA_R6 E12
VGA_R5 D12
D6
C5
VGA_B2 H13
VGA_G2 H12
IO_8A/DIFFIO_TX_T2P/DQ1T
IO_8A/DIFFIO_TX_T2N/DQ1T
IO_8A/DIFFIO_RX_T3P/DQ1T
IO_8A/DIFFIO_RX_T3N/DQ1T
IO_8A/DIFFIO_RX_T5P/DQS1T
IO_8A/DIFFIO_RX_T5N/DQSN1T
IO_8A/DIFFIO_RX_T6P
IO_8A/DIFFIO_RX_T6N/DQ1T
IO_8A/DIFFIO_RX_T7P/DQ1T
IO_8A/DIFFIO_RX_T7N/DQ1T
IO_8A/DIFFIO_TX_T8P/DQ1T
IO_8A/DIFFIO_TX_T8N
IO_8A/DIFFIO_TX_T10P/DQ2T
IO_8A/DIFFIO_RX_T10N/DQ2T
IO_8A/DIFFIO_RX_T11P/DQ2T
IO_8A/DIFFIO_RX_T11N/DQ2T
IO_8A/DIFFIO_RX_T12P/DQ2T
IO_8A/DIFFIO_RX_T12N/DQ2T
IO_8A/DIFFIO_RX_T13P/DQS2T
IO_8A/DIFFIO_RX_T13N/DQSN2T
IO_8A/DIFFIO_TX_T14P
IO_8A/DIFFIO_TX_T14N/DQ2T
IO_8A/DIFFIO_RX_T15P/DQ2T
IO_8A/DIFFIO_RX_T15N/DQ2T
IO_8A/DIFFIO_TX_T16P/DQ2T
IO_8A/DIFFIO_TX_T16N
IO_8A/DIFFIO_RX_T17P
IO_8A/DIFFIO_RX_T17N
IO_8A/DIFFIO_TX_T18P/DQ3T
IO_8A/DIFFIO_RX_T18N/DQ3T
IO_8A/DIFFIO_RX_T19P/DQ3T
IO_8A/DIFFIO_RX_T19N/DQ3T
IO_8A/DIFFIO_TX_T20P/DQ3T
IO_8A/DIFFIO_TX_T20N/DQ3T
IO_8A/DIFFIO_RX_T21P/DQS3T
IO_8A/DIFFIO_RX_T21N/DQSN3T
IO_8A/DIFFIO_TX_T22P
IO_8A/DIFFIO_TX_T22N/DQ3T
IO_8A/DIFFIO_RX_T23P/DQ3T
IO_8A/DIFFIO_RX_T23N/DQ3T
IO_8A/DIFFIO_TX_T24P/DQ3T
IO_8A/DIFFIO_TX_T24N
IO_8A/DIFFIO_RX_T25P
IO_8A/DIFFIO_RX_T25N
IO_8A/DIFFIO_TX_T26P/DQ4T
IO_8A/DIFFIO_TX_T26N/DQ4T
IO_8A/DIFFIO_RX_T27P/DQ4T
IO_8A/DIFFIO_RX_T27N/DQ4T
IO_8A/DIFFIO_TX_T28P/DQ4T
IO_8A/DIFFIO_TX_T28N/DQ4T
IO_8A/DIFFIO_RX_T29P/DQS4T
IO_8A/DIFFIO_RX_T29N/DQSN4T
IO_8A/DIFFIO_TX_T30P
IO_8A/DIFFIO_TX_T30N/DQ4T
IO_8A/DIFFIO_RX_T31P/DQ4T
IO_8A/DIFFIO_RX_T31N/DQ4T
IO_8A/DIFFIO_TX_T32P/DQ4T
IO_8A/DIFFIO_TX_T32N
IO_8A/DIFFIO_RX_T33P
IO_8A/DIFFIO_RX_T33N
IO_8A/DIFFIO_TX_T34P/DQ5T
IO_8A/DIFFIO_TX_T34N/DQ5T
IO_8A/DIFFIO_RX_T35P/DQ5T
IO_8A/DIFFIO_RX_T35N/DQ5T
IO_8A/DIFFIO_TX_T36P/DQ5T
IO_8A/DIFFIO_TX_T36N/DQ5T
IO_8A/DIFFIO_RX_T37P/DQS5T
IO_8A/DIFFIO_RX_T37N/DQSN5T
IO_8A/DIFFIO_TX_T38P
IO_8A/DIFFIO_TX_T38N/DQ5T
IO_8A/DIFFIO_RX_T39P/DQ5T
IO_8A/DIFFIO_RX_T39N/DQ5T
IO_8A/DIFFIO_TX_T40P/DQ5T
IO_8A/DIFFIO_TX_T40N
D5
C4
F11 VGA_G6
E11 VGA_G7
E8
D7
J7 18 AUD_DACDAT
H7 18 AUD_BCLK
B2 TD_DATA3
B1 TD_DATA1
B6
B5
C3
B3 TD_DATA7
K12 26 FPGA_I2C_SDAT
J12 26 FPGA_I2C_SCLK
D2 TD_DATA0
C2 TD_DATA6
G12 VGA_G5
G11 VGA_G4
E4
D4
K7 18 AUD_ADCDAT
K8 18 AUD_ADCLRCK
E3
E2 TD_DATA2
G10 VGA_G3
F10 16 VGA_BLANK_N
E1 TD_DATA5
D1 TD_DATA4
J10 VGA_G1
J9 VGA_G0
E7
E6
F9
F8
G7 18 AUD_XCK
F6 17 TD_RESET_N
5CSEMA5F31
Default Setting: BOOTSEL[2:0]=101 (Boot from SD CARD)
CLKSEL[1:0]=0
VCC3P3
SW16 DNI
R105 1K
R104 1K
R103 1K
R96 1K
R95 1K
HPS_BOOTSEL0 (BOOTSEL0) R108 10K
HPS_FLASH_NCSO (BOOTSEL1) R107 10K DNI
HPS_BOOTSEL2 (BOOTSEL2) R106 10K
HPS_SPIM_SS (CLOCKSEL0) R98 10K DNI
HPS_CLOCKSEL1 (CLOCKSEL1) R97 10K DNI
SW-DIP12
DNI R111 1K
R110 1K
DNI R109 1K
R100 1K
R99 1K
HPS_BOOTSEL0 (BOOTSEL0)
HPS_FLASH_NCSO (BOOTSEL1)
HPS_BOOTSEL2 (BOOTSEL2)
HPS_SPIM_SS (CLOCKSEL0)
HPS_CLOCKSEL1 (CLOCKSEL1)
Copyright (c) 2013 by Terasic Technologies Inc. Taiwan.
All rights reserved.
No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.
Title
DE1-SoC Board
Size B
Document Number
FPGA BANK 7, BANK 8
Rev C
Date: Monday, March 24, 2014
Sheet 5 of 30



Title: **DE1-SoC Board**

Size	Document Number	Rev
B	FPGA Clocks & GND	C

Date: Monday, March 24, 2014 Sheet 6 of 30

USB Blaster

FPGA_TDI 11
JTAG_TMS 11
JTAG_TCK 11
FPGA_TDO 11

R141 0 DNI JTAG_TCK
C73 33p 50V DNI
R142 1K

Design Note:
Optional termination resistor for DCLK

CAD Note:
Place near FPGA DCLK pin

VCC3P3
R146 10K DNI
R147 0 DNI
C82 12p 50V DNI
R145 1K DNI

U20-1

Configuration

Bank 3A VCCIO = 3.3V

TCK	JTAG_TCK AC5
TMS	JTAG_TMS V9
TDO	FPGA_TDO AB9
TDI	FPGA_TDI U8
DCLK	EPCQ_DCLK U7
AS_DATA0,ASDO/DATA0	EPCQ_AS_DATA0 AE6
AS_DATA1/DATA1	EPCQ_AS_DATA1 AE5
AS_DATA2/DATA2	EPCQ_AS_DATA2 AE8
AS_DATA3/DATA3	EPCQ_AS_DATA3 AC7
NCSO/DATA4	EPCQ_NCSO AB8
IO_3A/DATA5/DIFFIO_TX_B2N	PS2_DAT2 21 AE9
IO_3A/DATA6/DIFFIO_RX_B1N/DQ1B	SW9 AE12
IO_3A/DATA7/DIFFIO_TX_B2P/DQ1B	PS2_CLK2 21 AD9
IO_3A/DATA8/DIFFIO_RX_B1P/DQ1B	SW4 AD11
IO_3A/DATA9/DIFFIO_TX_B4N/DQ1B	SW3 AF10
IO_3A/DATA10/DIFFIO_RX_B3N/DQSN1B	SW8 AD10
IO_3A/DATA11/DIFFIO_TX_B4P	SW6 AE11
IO_3A/DATA12/DIFFIO_RX_B3P/DQS1B	SW7 AC9
IO_3A/DATA13/DIFFIO_TX_B6N/DQ1B	AH4
IO_3A/DATA14/DIFFIO_RX_B5N/DQ1B	PS2_DAT 21 AE7
IO_3A/DATA15/DIFFIO_TX_B6P/DQ1B	AG3
IO_3A/CLKUSR/DIFFIO_RX_B5P/DQ1B	PS2_CLK 21 AD7

Bank 5A VCCIO = 3.3V

IO_5A/INIT_DONE/DIFFIO_RX_R2P	AD25 HEX32
IO_5A/CRC_ERROR/DIFFIO_RX_R2N	AC25 HEX33
IO_5A/DEV_OE/DIFFIO_TX_R5P	AE26 HEX00
IO_5A/NCEO/DIFFIO_TX_R3P/DQ1R	AJ29 HEX10
IO_5A/DEV_CLRN/DIFFIO_TX_R5N/DQ1R	AD27 HEX16

Bank 9A

CONF_DONE	R118 10K FPGA_CONF_DONE F3
NSTATUS	R117 10K FPGA_NSTATUS F4
NCONFIG	R119 10K FPGA_NCONFIG J5
NCE	G5
MSEL0	L8 MSEL0
MSEL1	K6 MSEL1
MSEL2	G6 MSEL2
MSEL3	L7 MSEL3
MSEL4	L9 MSEL4

5CSEMA5F31

VCC3P3_PGM

FPGA_NCONFIG 10
FPGA_CONF_DONE 10

SW[9..0] 3,20

HEX0[6..0] 4,19
HEX1[6..0] 4,19
HEX3[6..0] 4,19

VCC12
J16 DNI
Power - FAN
FAN_CTRL 3
Q5 FDV305N DNI
D99 SM2T3V3A 3.3V 200W DNI

Fix MSEL[4:0]=10010 in AS Fast Mode

SW10 SW-DIP12
VCC3P3_PGM
MSEL0 R136 1K
MSEL1 R135 1K
MSEL2 R122 1K
MSEL3 R121 1K
MSEL4 R120 1K

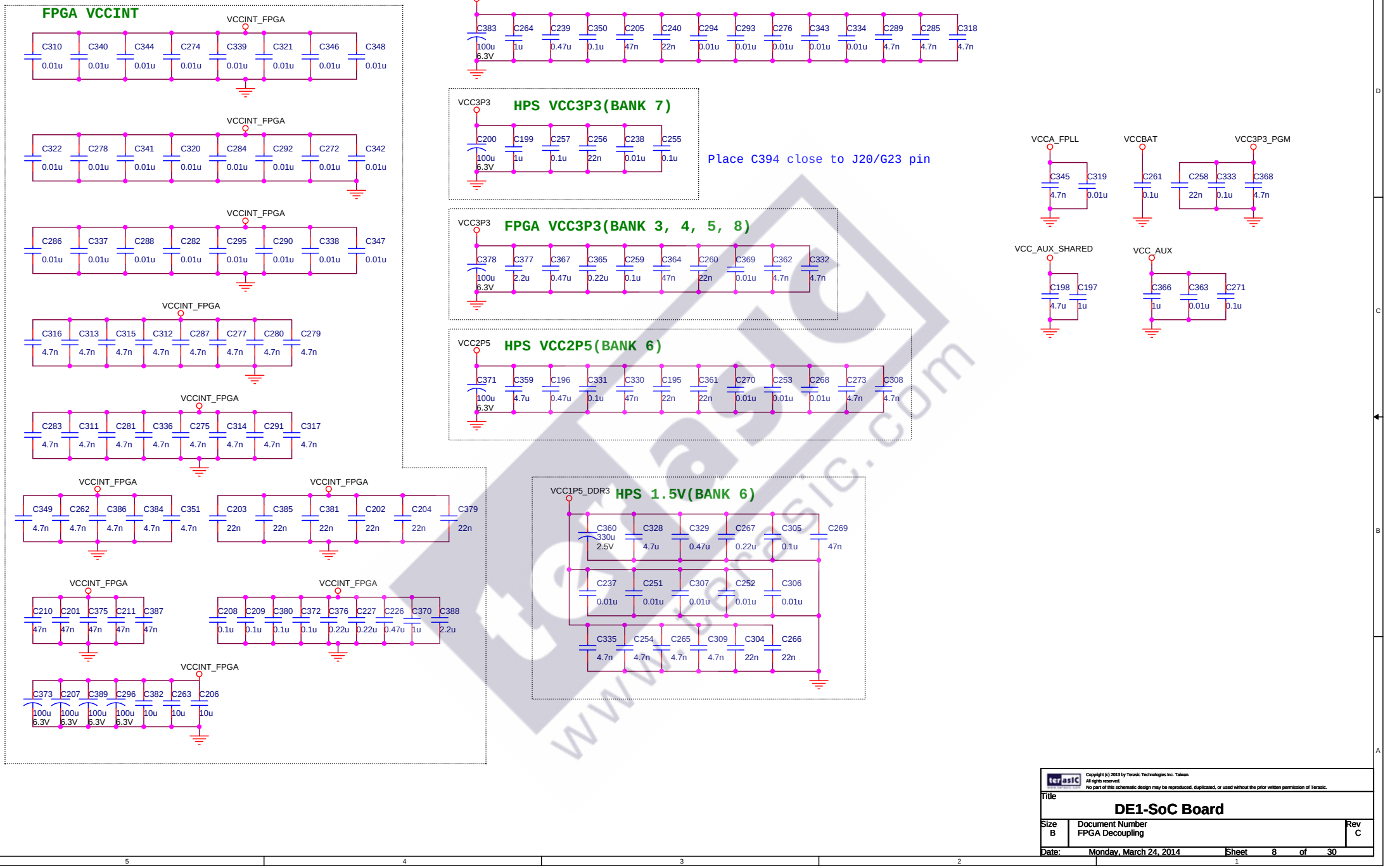
R138 0 DNI MSEL0
R137 0 DNI MSEL1
R125 0 DNI MSEL2
R124 0 DNI MSEL3
R123 0 DNI MSEL4

VCC3P3
U40 EPCQ256
C105 0.1u 10V
NC01 NC02 NC03 NC04 NC05 NC06 NC07 NC08
VCC GND
DATA0 DATA1 DATA2 DATA3 DCLK nCS
EPCQ_AS_DATA0
EPCQ_AS_DATA1
EPCQ_AS_DATA2
EPCQ_AS_DATA3
EPCQ_DCLK
EPCQ_NCSO

Title: **DE1-SoC Board**

Size	Document Number	Rev
B	FPGA Configuration	C

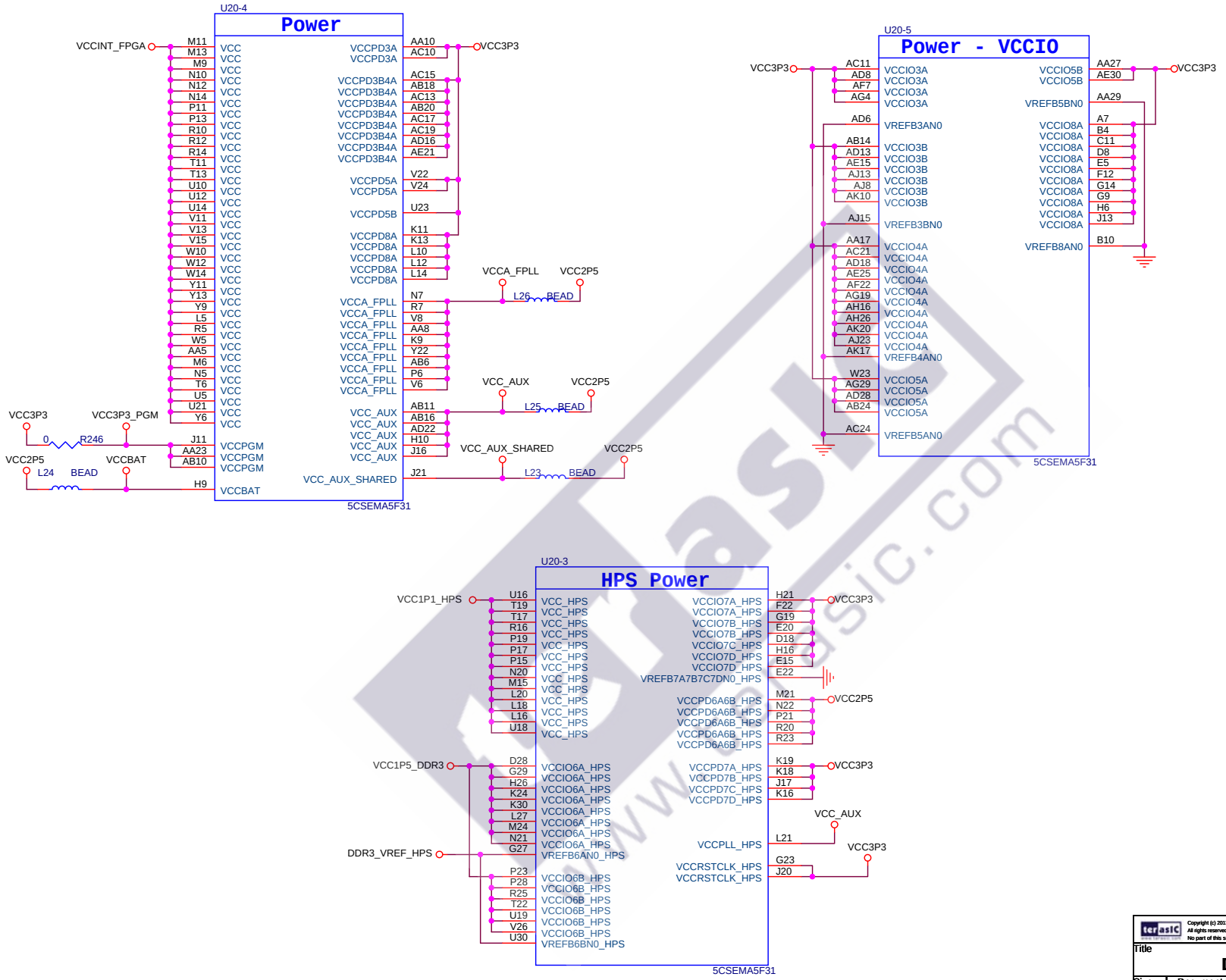
Date: Monday, March 24, 2014 Sheet 7 of 30



Title: **DE1-SoC Board**

Size	Document Number	Rev
B	FPGA Decoupling	C

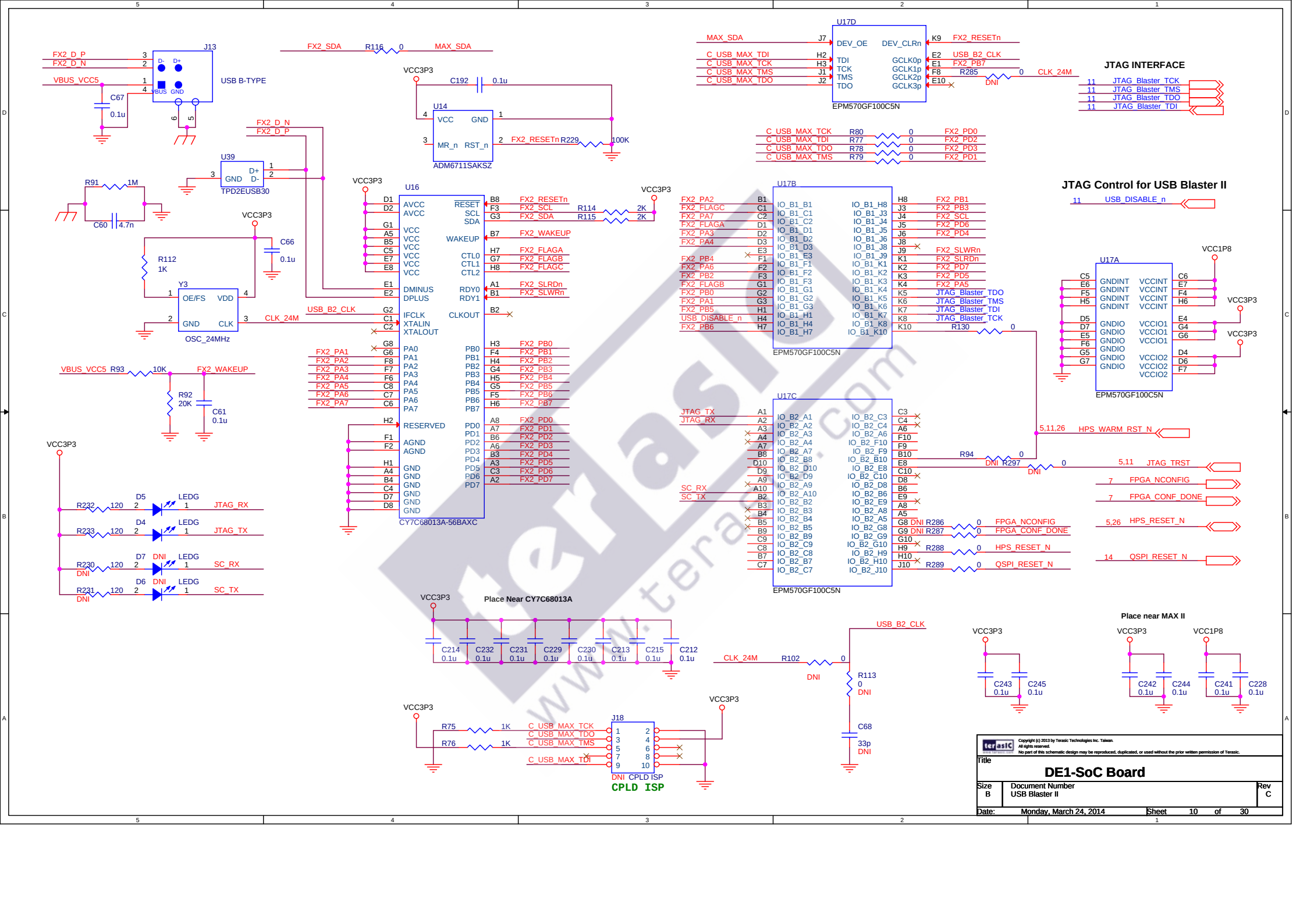
Date: Monday, March 24, 2014 Sheet 8 of 30

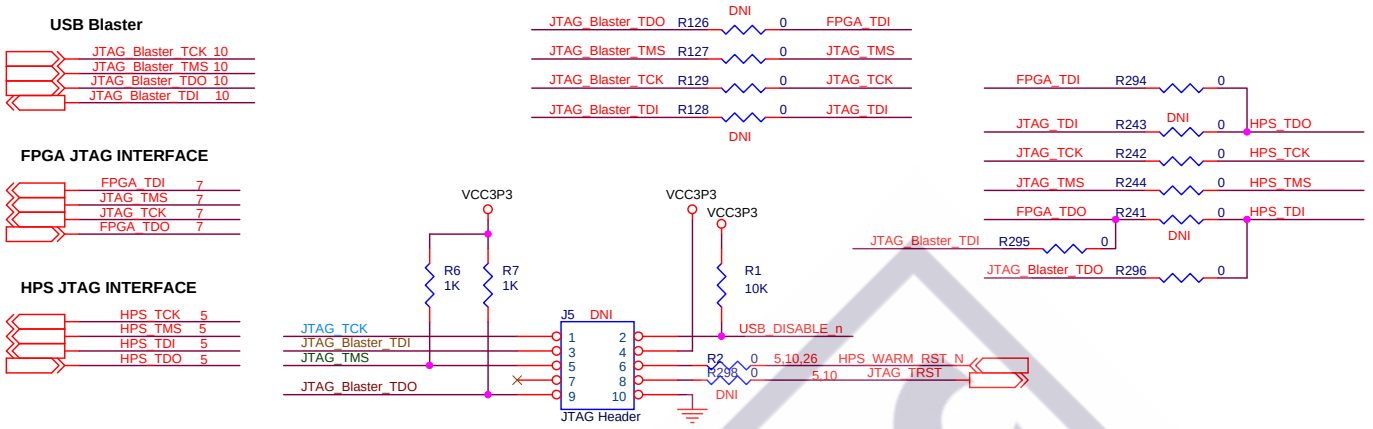


Title
DE1-SoC Board

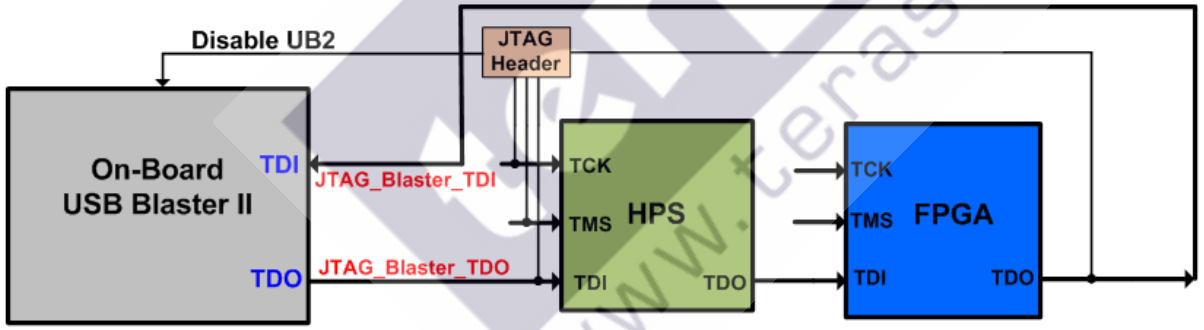
Size	Document Number	Rev
B	FPGA Power	C

Date: Monday, March 24, 2014 Sheet 9 of 30


JTAG INTERFACE
JTAG Control for USB Blaster II
Place Near CY7C68013A
Place near MAX II
CPLD ISP
USB B-TYPE
TPD2EUSB30
ADM6711SAKSZ
OSC_24MHz
CY7C68013A-56BAXC
EPM570GF100C5N
JTAG_Blaster_TCK
JTAG_Blaster_TMS
JTAG_Blaster_TDO
JTAG_Blaster_TDI
USB_DISABLE_n
HPS_WARM_RST_N
JTAG_TRST
FPGA_NCONFIG
FPGA_CONF_DONE
HPS_RESET_N
QSPI_RESET_N
DE1-SoC Board
USB Blaster II
Monday, March 24, 2014
Sheet 10 of 30
Rev C



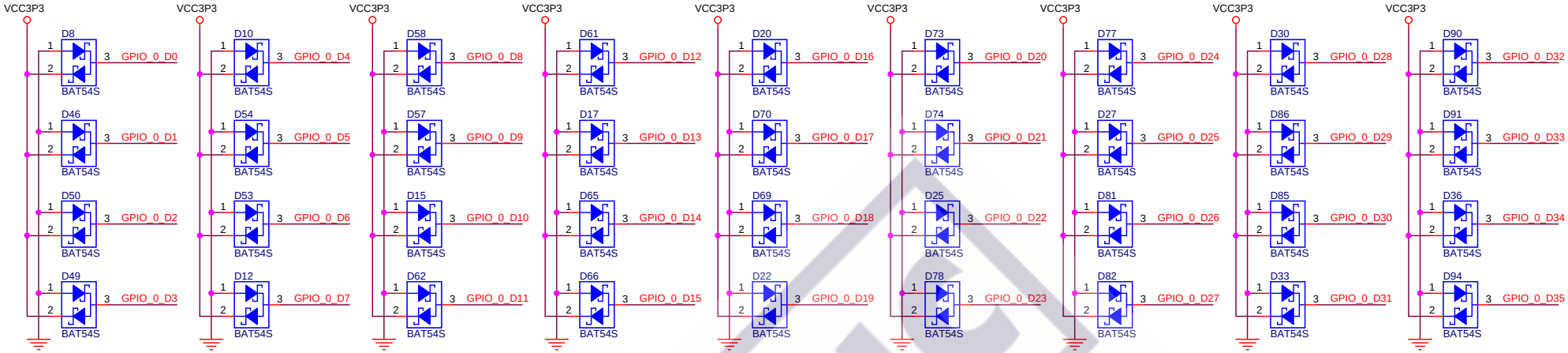
JTAG Chain



Title: **DE1-SoC Board**

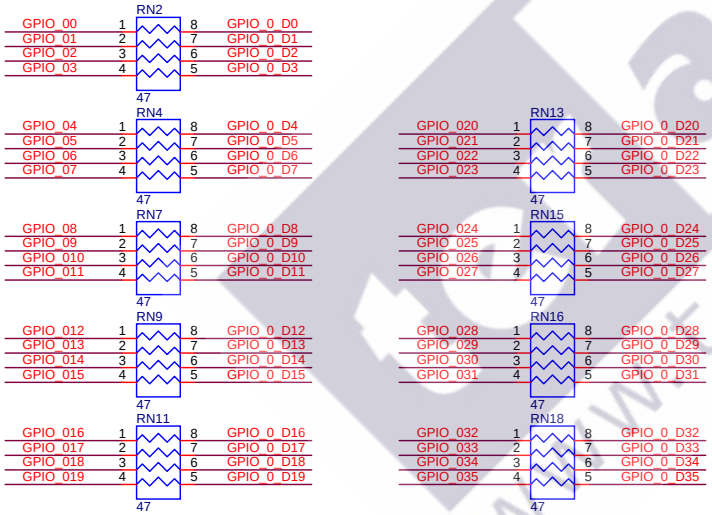
Size	Document Number	Rev
B	JTAG Chain	C

Date: Monday, March 24, 2014 Sheet 11 of 30

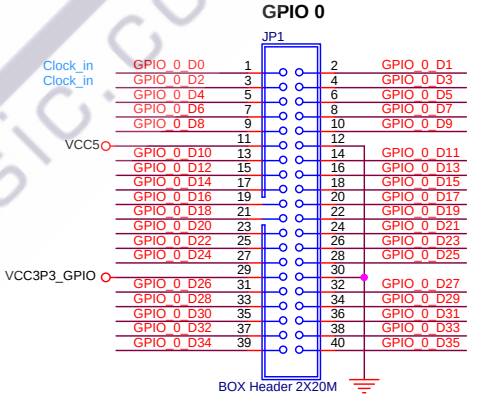


GPIO 0

GPIO_0[35..0] 3,6



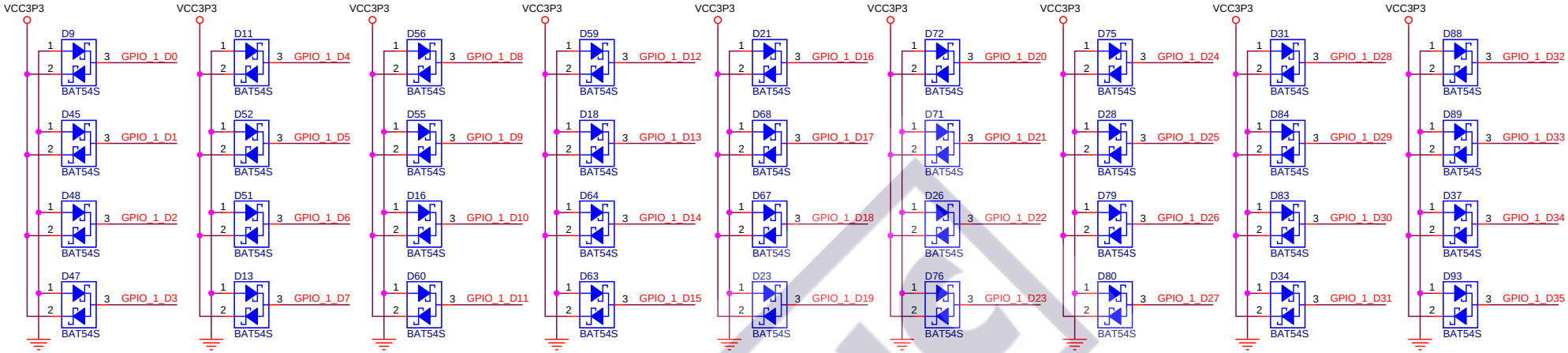
GPIO 0



Title: **DE1-SoC Board**

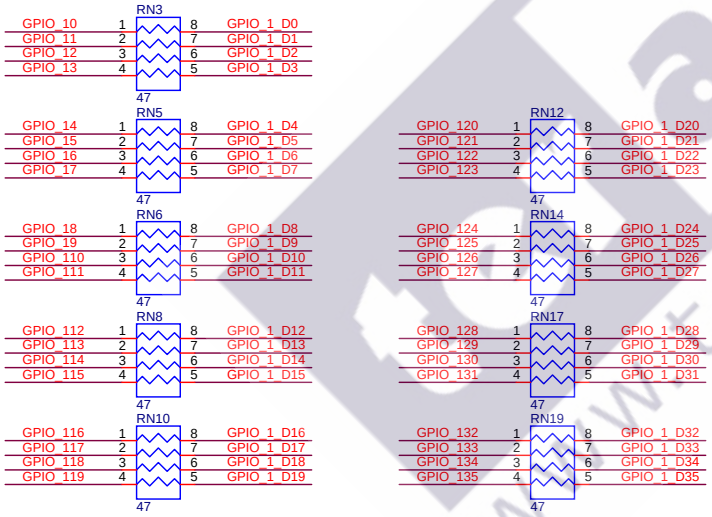
Size	Document Number	Rev
B	GPIO 0	C

Date: Monday, March 24, 2014 Sheet 12 of 30

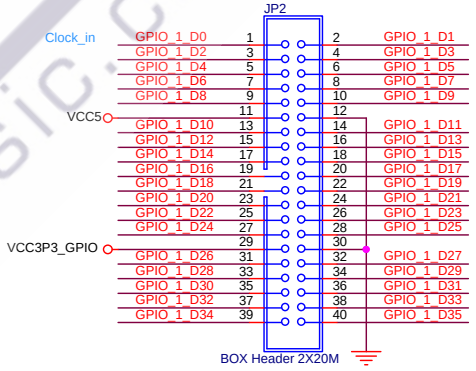


GPIO 1

GPIO_1[35..0] 3,6



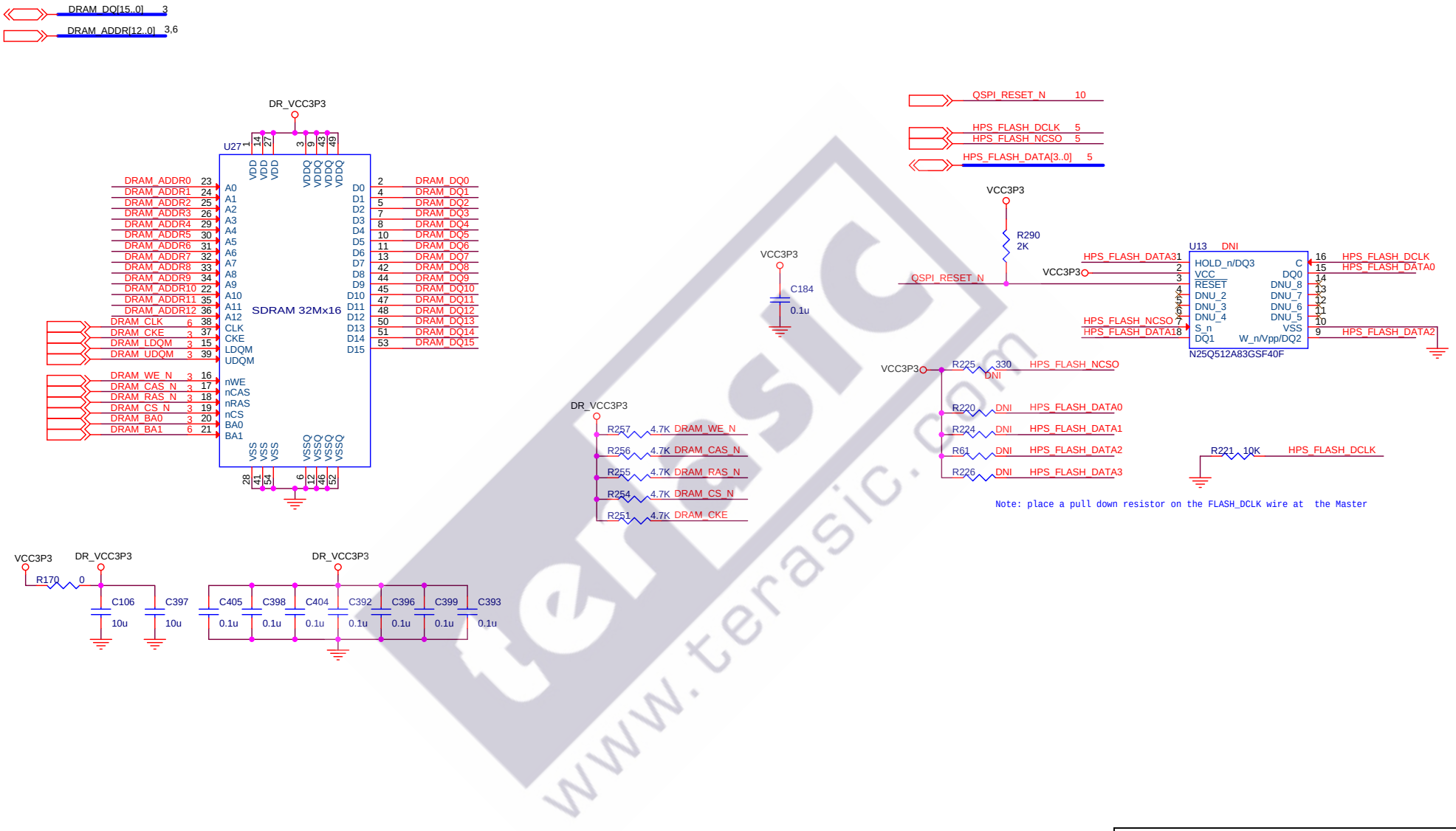
GPIO 1



Title: **DE1-SoC Board**

Size	Document Number	Rev
B	GPIO 1	C

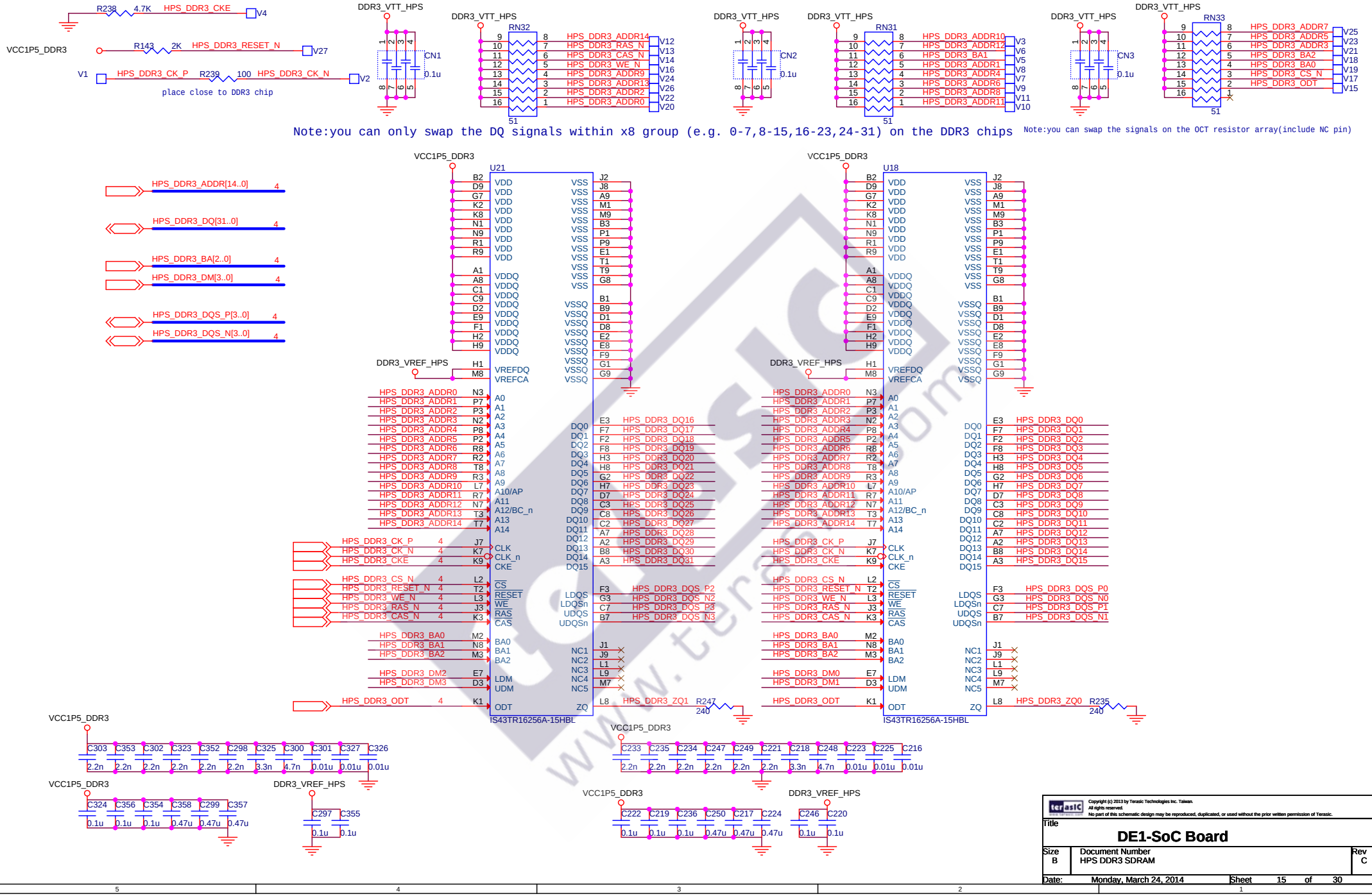
Date: Monday, March 24, 2014 Sheet 13 of 30



Title: **DE1-SoC Board**

Size	Document Number	Rev
B	SDRAM & HPS QSPI Flash	C

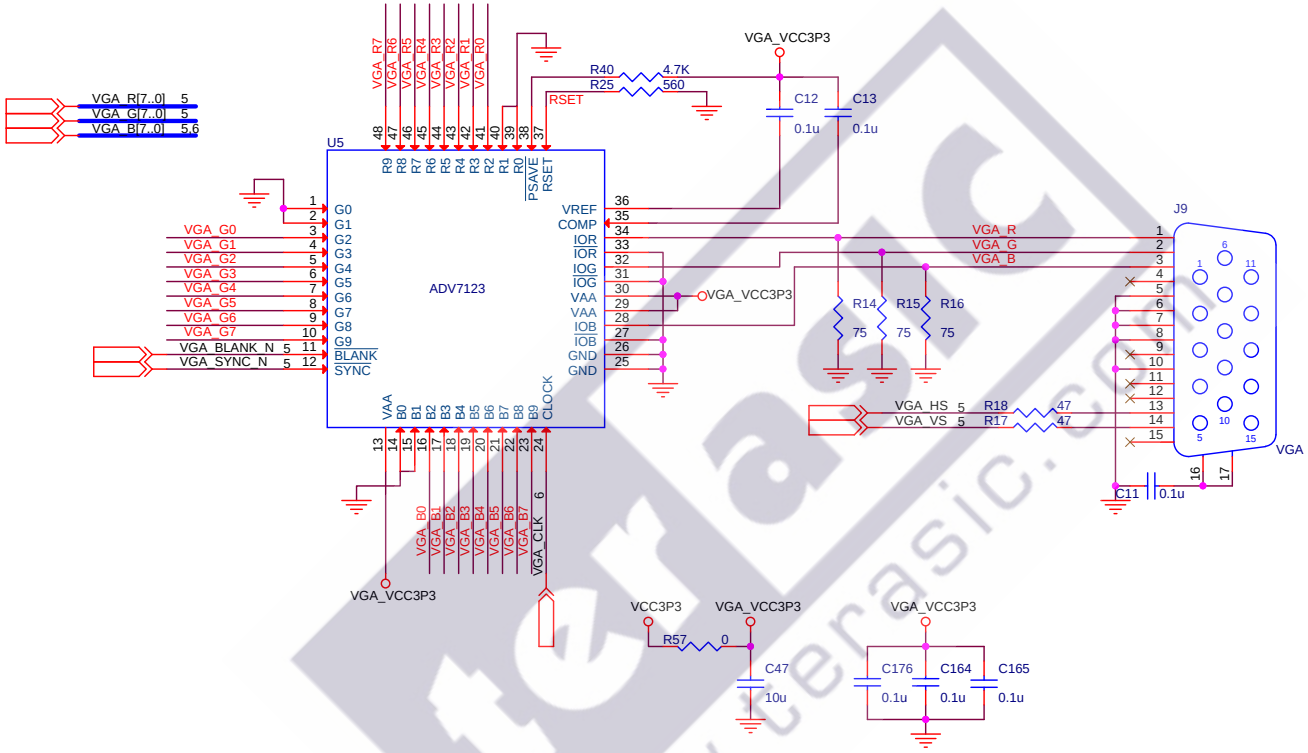
Date: Monday, March 24, 2014 Sheet 14 of 30



Title
DE1-SoC Board

Size	Document Number	Rev
B	HPS DDR3 SDRAM	C

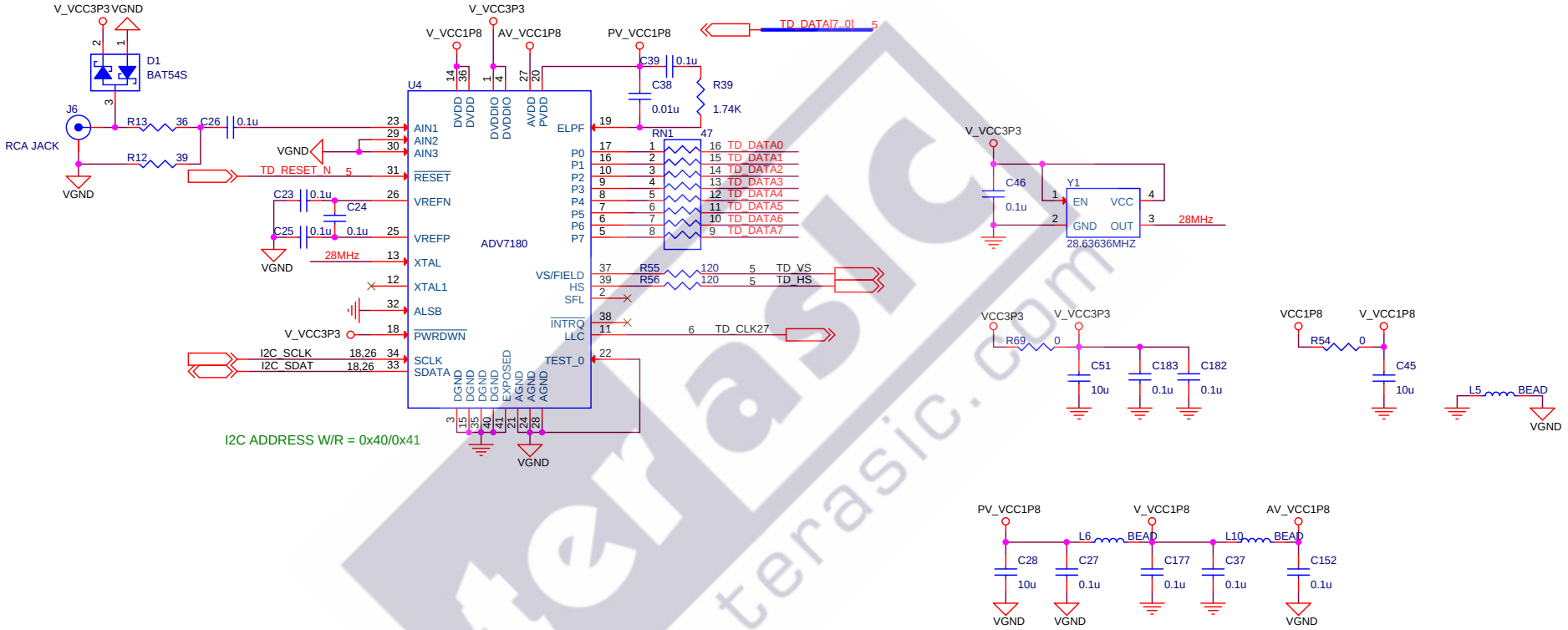
Date: Monday, March 24, 2014 Sheet 15 of 30



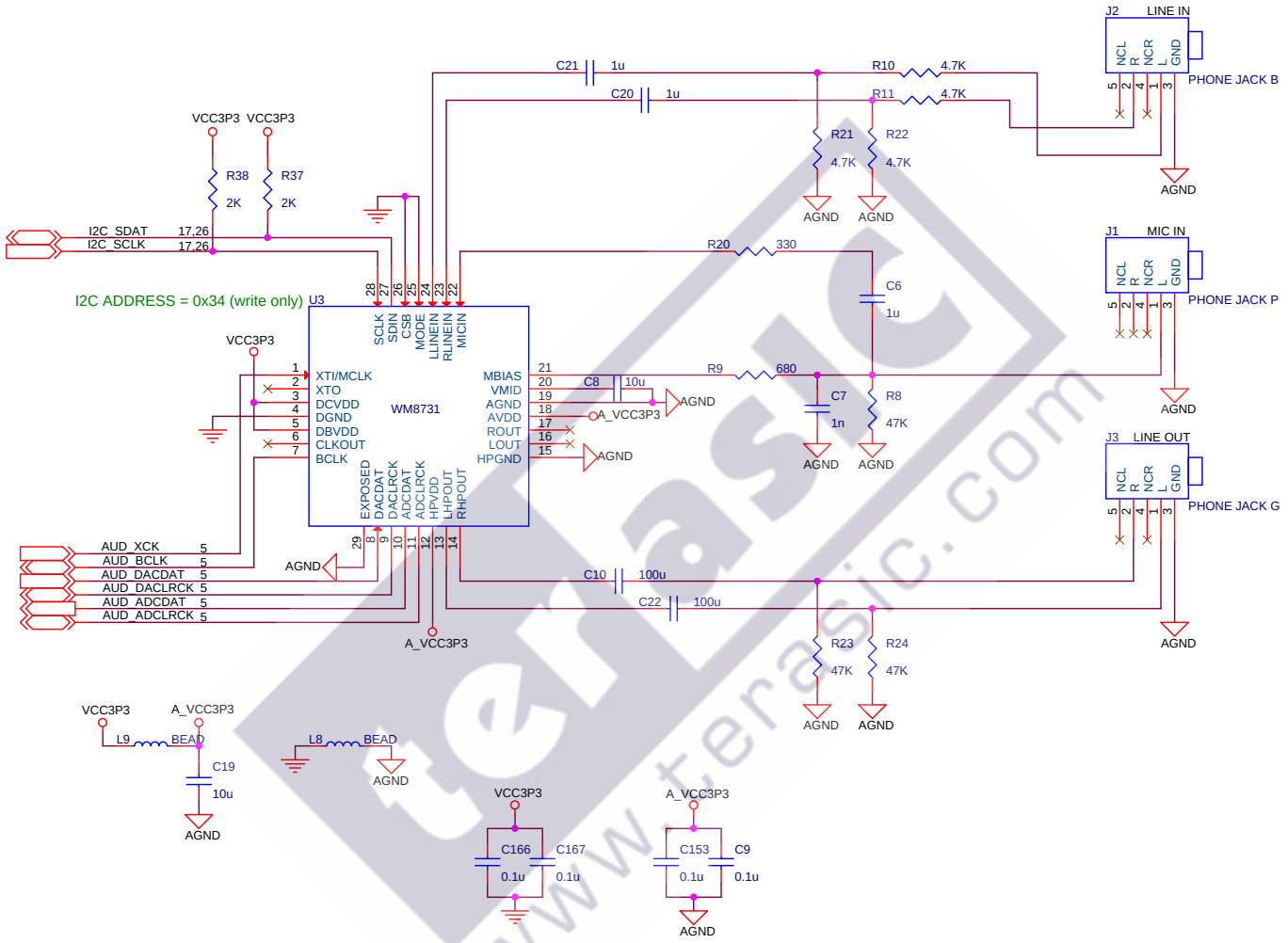
Title
DE1-SoC Board

Size	Document Number	Rev
B	ADV7123 VGA	C

Date: Monday, March 24, 2014 Sheet 16 of 30



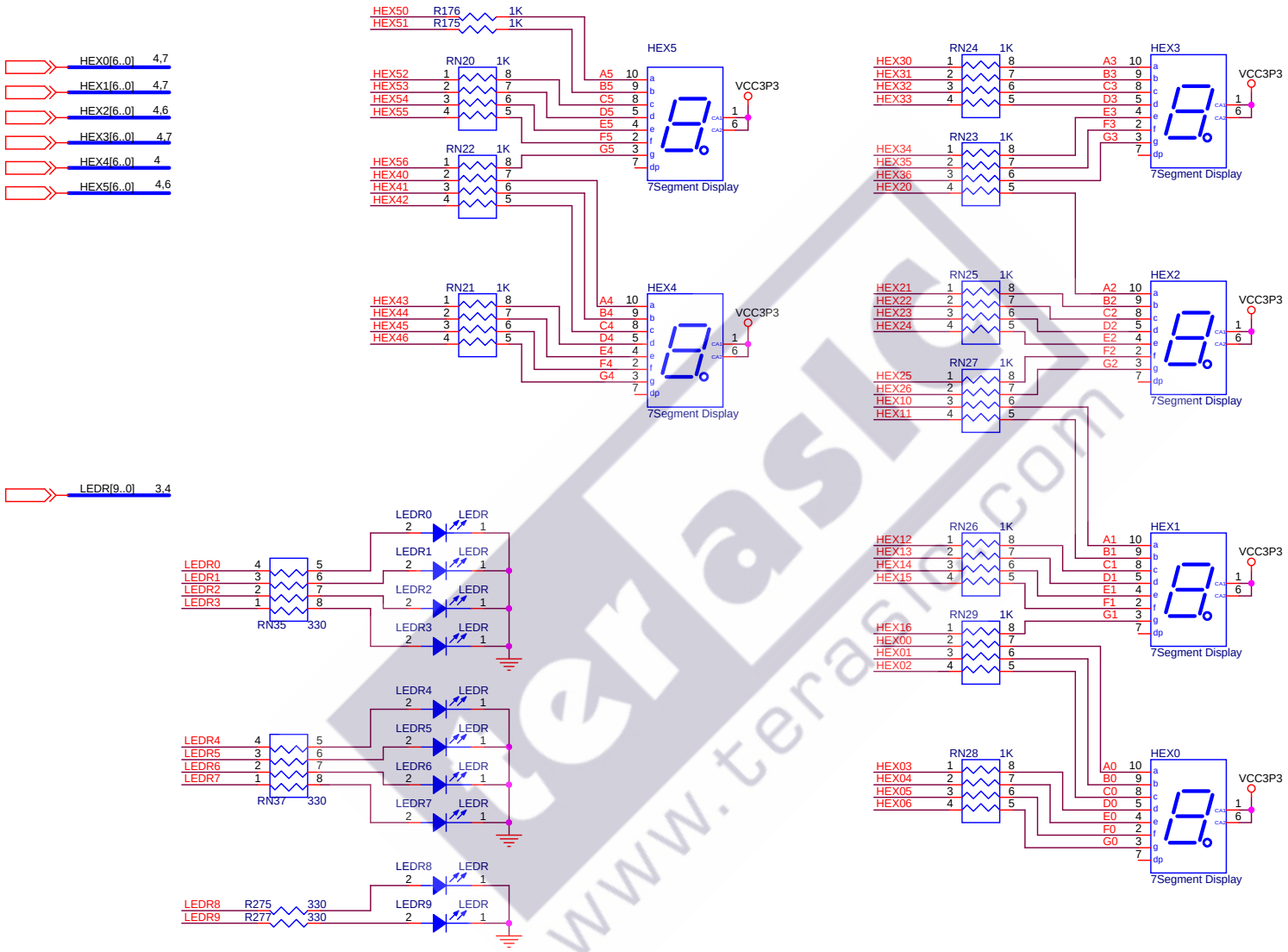
Title	DE1-SoC Board	
Size B	Document Number ADV7180 Video Decoder	Rev C
Date: Monday, March 24, 2014	Sheet 17 of 30	



Title
DE1-SoC Board

Size	Document Number	Rev
B	Audio CODEC	C

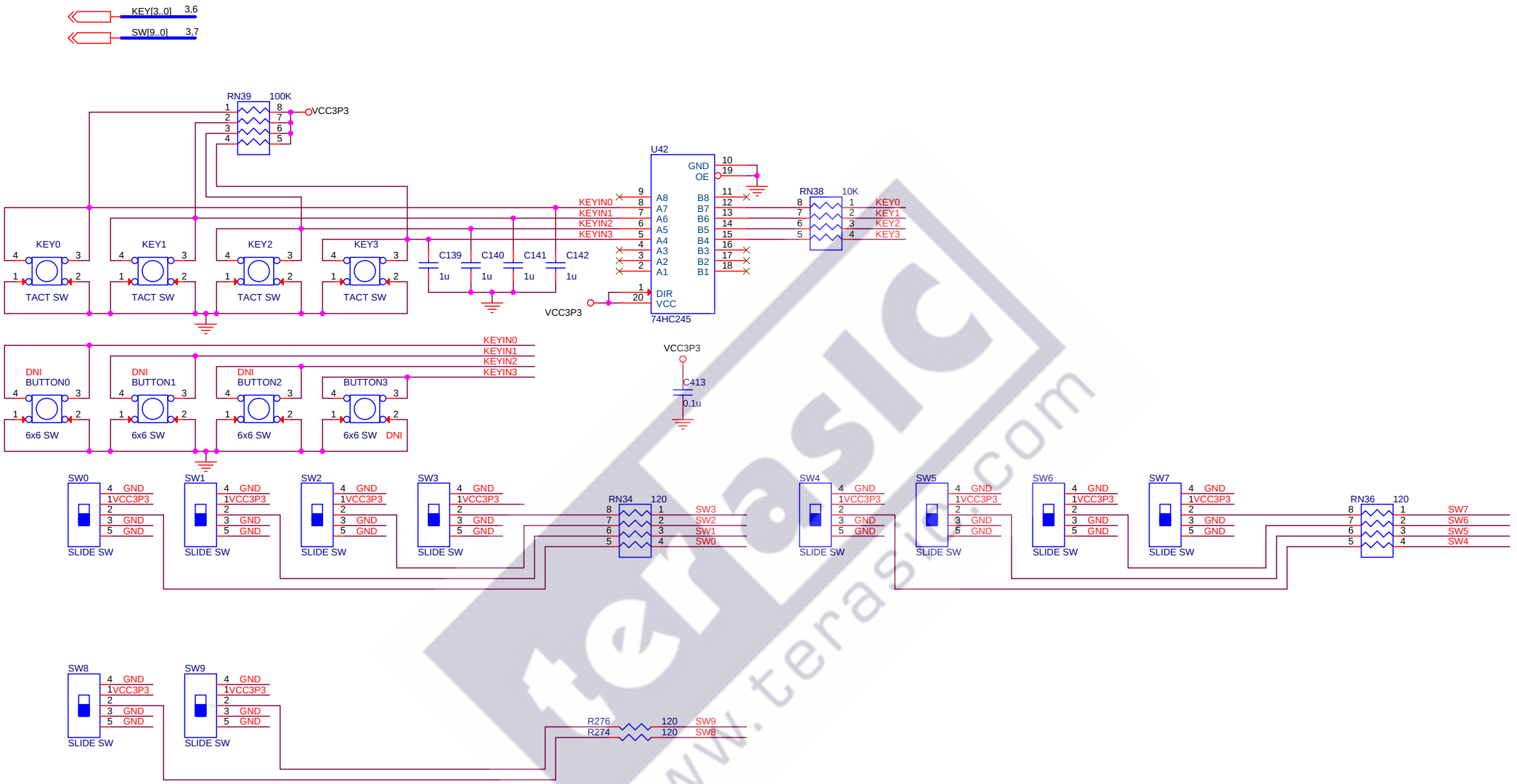
Date: Monday, March 24, 2014 Sheet 18 of 30



Title
DE1-SoC Board

Size	Document Number	Rev
B	7-Segment Display, LED	C

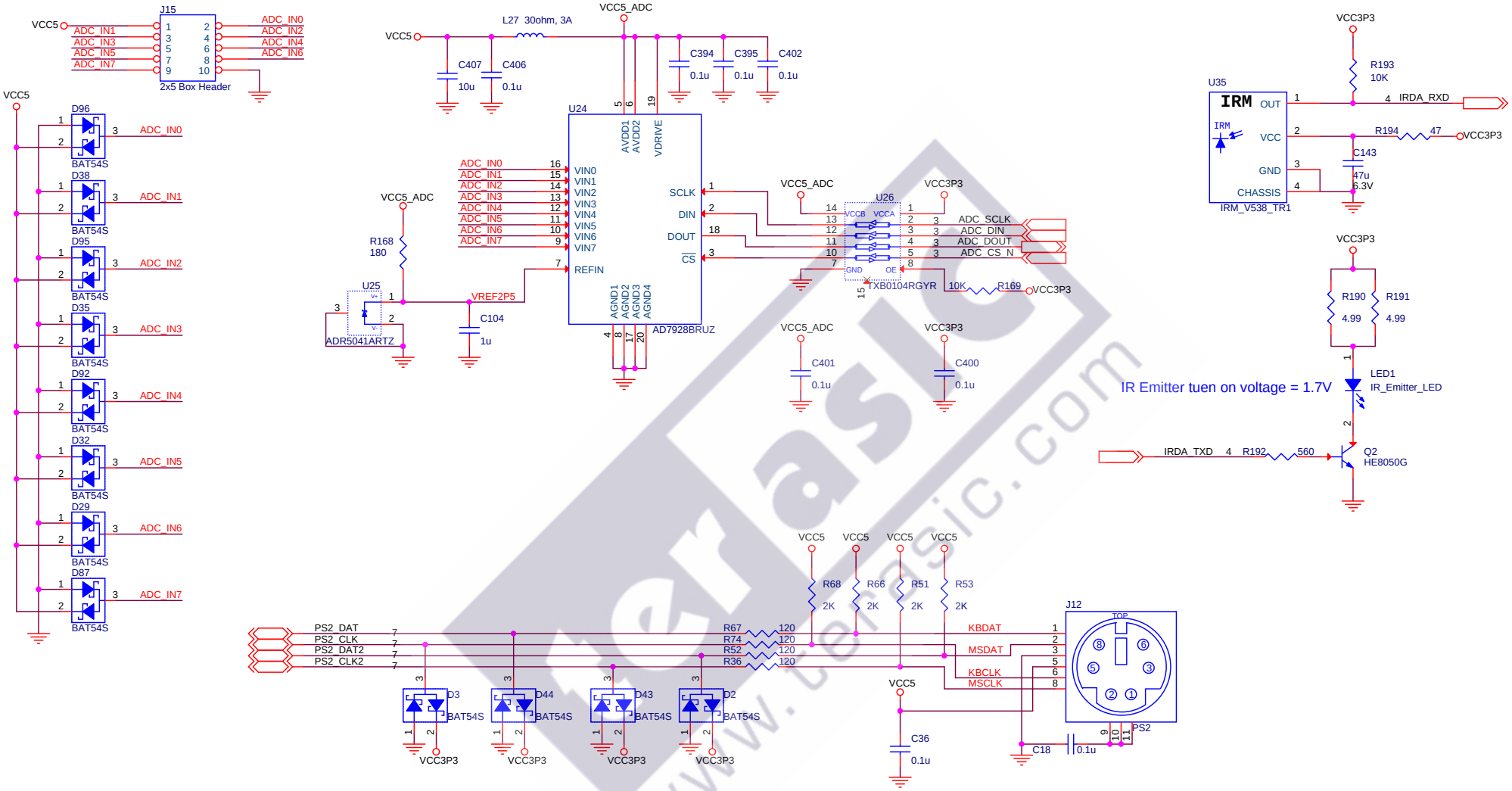
Date: Monday, March 24, 2014 Sheet 19 of 30



Title
DE1-SoC Board

Size	Document Number	Rev
B	FPGA BUTTON, Switch	C

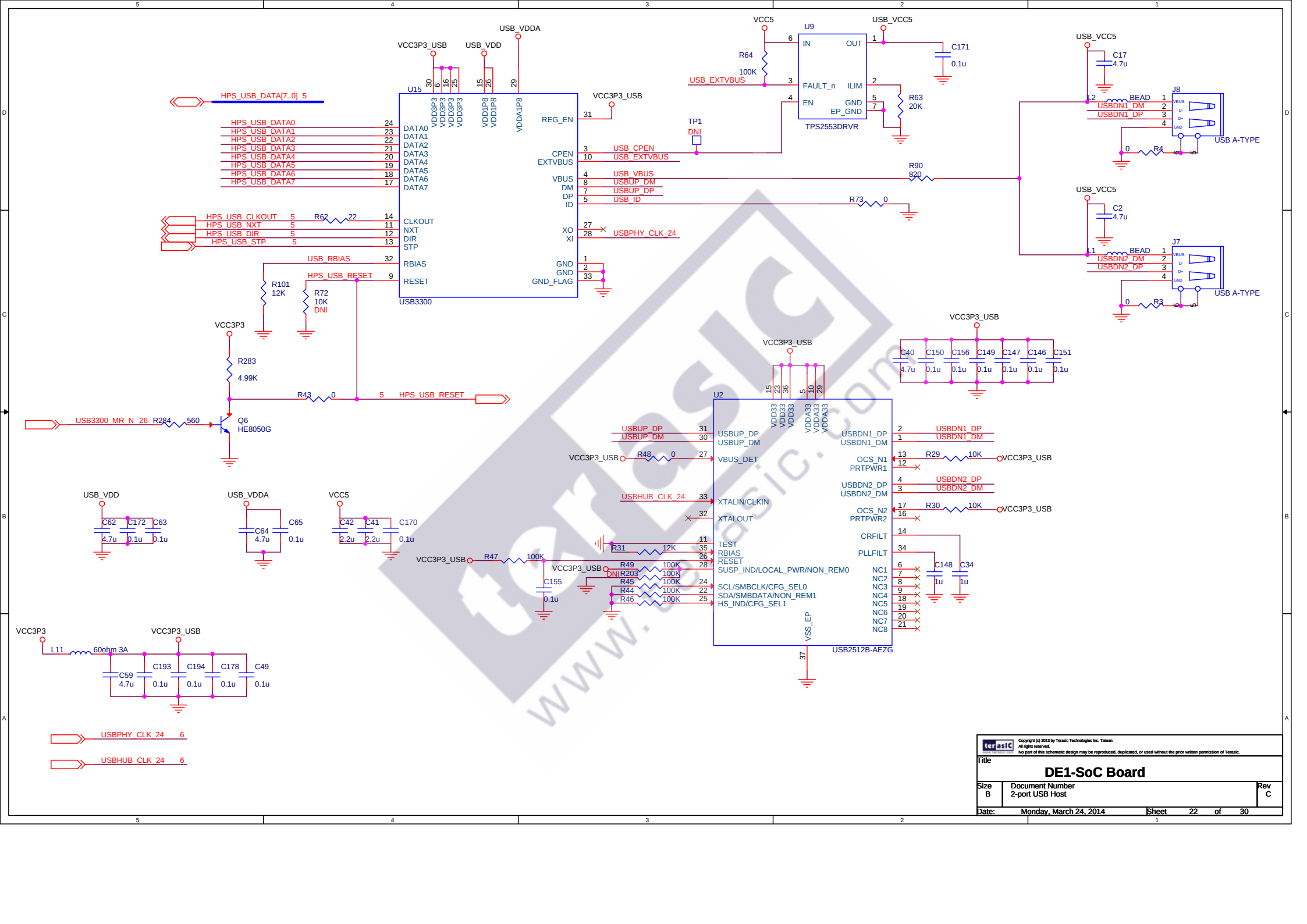
Date: Monday, March 24, 2014 Sheet 20 of 30



Title: **DE1-SoC Board**

Size	Document Number	Rev
B	ADC, PS2, IR Tx, IR Rx	C

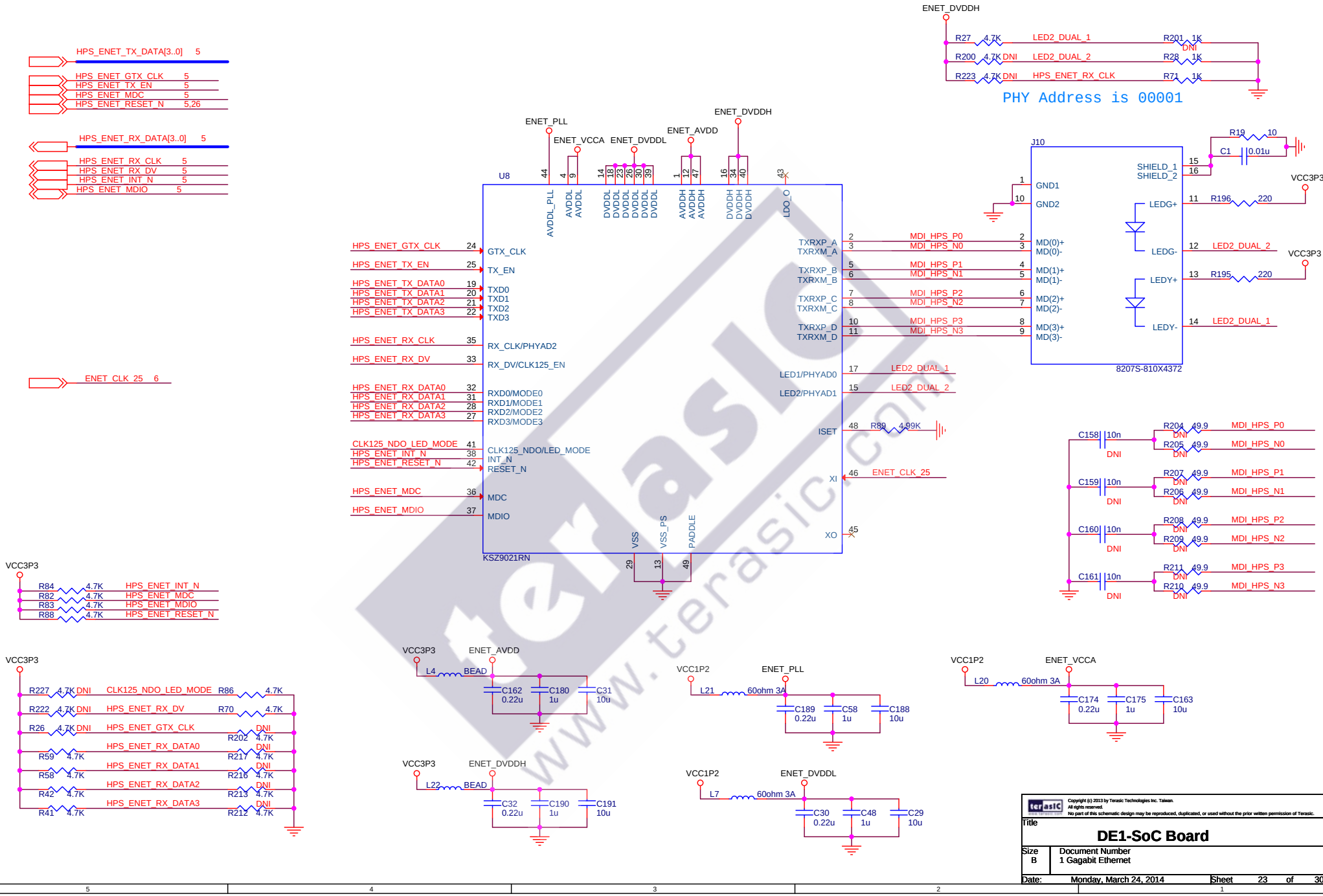
Date: Monday, March 24, 2014 Sheet 21 of 30

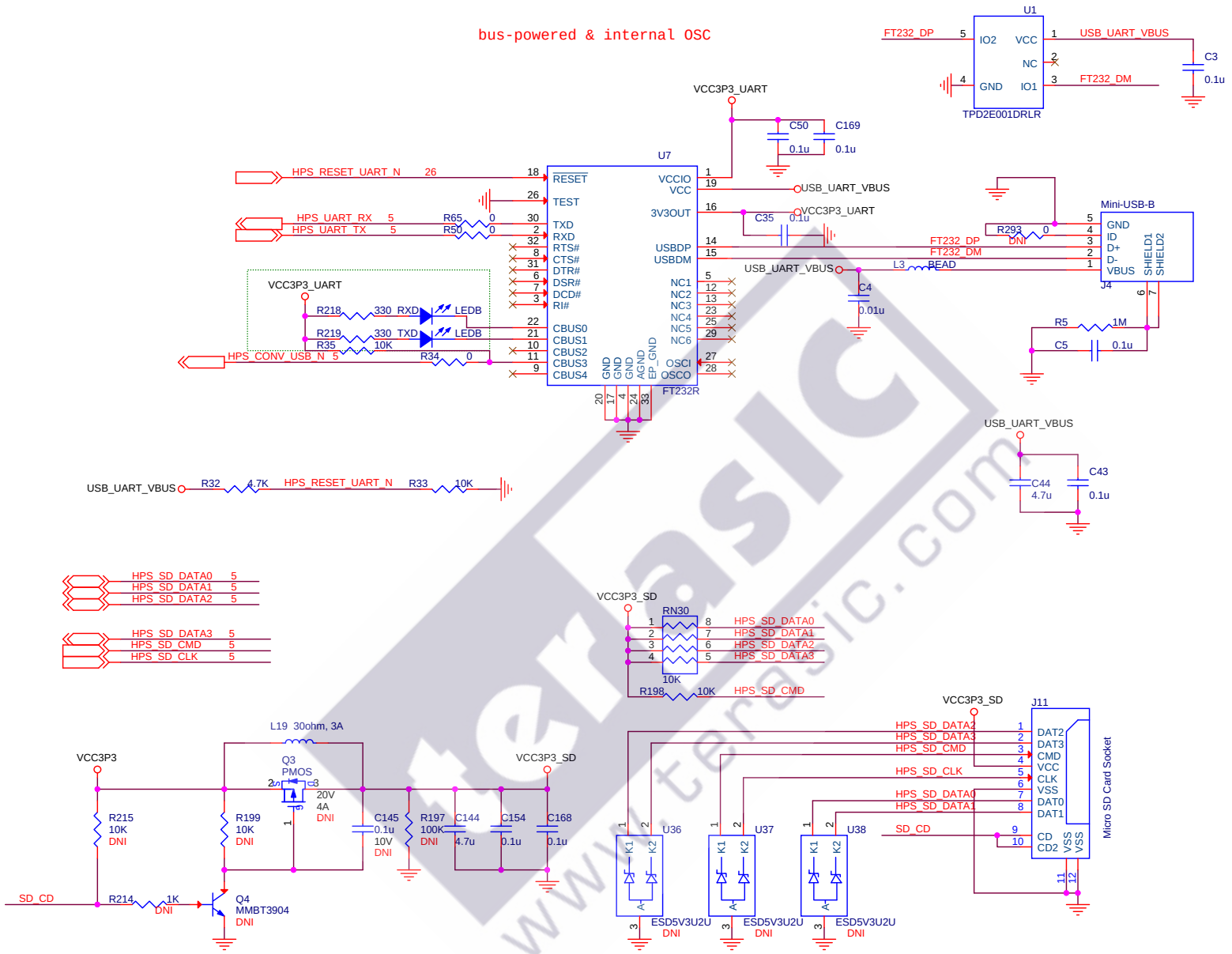


Title: **DE1-SoC Board**

Size	Document Number	Rev
B	2-port USB Host	C

Date: Monday, March 24, 2014 Sheet 22 of 30


HPS_ENET_TX_DATA[3..0] 5
HPS_ENET_GTX_CLK 5
HPS_ENET_TX_EN 5
HPS_ENET_MDC 5
HPS_ENET_RESET_N 5,26
HPS_ENET_RX_DATA[3..0] 5
HPS_ENET_RX_CLK 5
HPS_ENET_RX_DV 5
HPS_ENET_INT_N 5
HPS_ENET_MDIO 5
ENET_CLK_25 6
ENET_DVDDH
R27 4.7K LED2_DUAL_1 R201 1K DNI
R200 4.7K DNI LED2_DUAL_2 R28 1K
R223 4.7K DNI HPS_ENET_RX_CLK R71 1K
PHY Address is 00001
ENET_PLL
ENET_VCCA
ENET_DVDDL
ENET_AVDD
ENET_DVDDH
U8
AVDDL_PLL
AVDDL
AVDDL
DVDDL
DVDDL
DVDDL
DVDDL
DVDDL
AVDDH
AVDDH
AVDDH
DVDDH
DVDDH
DVDDH
LDO_O
HPS_ENET_GTX_CLK 24 GTX_CLK
HPS_ENET_TX_EN 25 TX_EN
HPS_ENET_TX_DATA0 19 TXD0
HPS_ENET_TX_DATA1 20 TXD1
HPS_ENET_TX_DATA2 21 TXD2
HPS_ENET_TX_DATA3 22 TXD3
HPS_ENET_RX_CLK 35 RX_CLK/PHYAD2
HPS_ENET_RX_DV 33 RX_DV/CLK125_EN
HPS_ENET_RX_DATA0 32 RXD0/MODE0
HPS_ENET_RX_DATA1 31 RXD1/MODE1
HPS_ENET_RX_DATA2 28 RXD2/MODE2
HPS_ENET_RX_DATA3 27 RXD3/MODE3
CLK125_NDO_LED_MODE 41 CLK125_NDO/LED_MODE
HPS_ENET_INT_N 38 INT_N
HPS_ENET_RESET_N 42 RESET_N
HPS_ENET_MDC 36 MDC
HPS_ENET_MDIO 37 MDIO
TXRXP_A
TXRXM_A
TXRXP_B
TXRXM_B
TXRXP_C
TXRXM_C
TXRXP_D
TXRXM_D
LED1/PHYAD0
LED2/PHYAD1
ISET
XI
XO
VSS
VSS_PS
PADDLE
KSZ9021RN
MDI_HPS_P0
MDI_HPS_N0
MDI_HPS_P1
MDI_HPS_N1
MDI_HPS_P2
MDI_HPS_N2
MDI_HPS_P3
MDI_HPS_N3
LED2_DUAL_1
LED2_DUAL_2
R89 4.99K
ENET_CLK_25
J10
GND1
GND2
MD(0)+
MD(0)-
MD(1)+
MD(1)-
MD(2)+
MD(2)-
MD(3)+
MD(3)-
SHIELD_1
SHIELD_2
LEDG+
LEDG-
LEDY+
LEDY-
R19 10
C1 0.01u
VCC3P3
R196 220
R195 220
8207S-810X4372
C158 10n DNI
C159 10n DNI
C160 10n DNI
C161 10n DNI
R204 49.9 DNI MDI_HPS_P0
R205 49.9 DNI MDI_HPS_N0
R207 49.9 DNI MDI_HPS_P1
R206 49.9 DNI MDI_HPS_N1
R208 49.9 DNI MDI_HPS_P2
R209 49.9 DNI MDI_HPS_N2
R211 49.9 DNI MDI_HPS_P3
R210 49.9 DNI MDI_HPS_N3
VCC3P3
R84 4.7K HPS_ENET_INT_N
R82 4.7K HPS_ENET_MDC
R83 4.7K HPS_ENET_MDIO
R88 4.7K HPS_ENET_RESET_N
R227 4.7K DNI CLK125_NDO_LED_MODE
R222 4.7K DNI HPS_ENET_RX_DV
R26 4.7K DNI HPS_ENET_GTX_CLK
R86 4.7K
R70 4.7K
R202 4.7K DNI
R59 4.7K HPS_ENET_RX_DATA0 DNI
R217 4.7K
R58 4.7K HPS_ENET_RX_DATA1 DNI
R216 4.7K
R42 4.7K HPS_ENET_RX_DATA2 DNI
R213 4.7K
R41 4.7K HPS_ENET_RX_DATA3 DNI
R212 4.7K
VCC3P3 ENET_AVDD
L4 BEAD
C162 0.22u
C180 1u
C31 10u
VCC1P2 ENET_PLL
L21 60ohm 3A
C189 0.22u
C58 1u
C188 10u
VCC1P2 ENET_VCCA
L20 60ohm 3A
C174 0.22u
C175 1u
C163 10u
VCC3P3 ENET_DVDDH
L22 BEAD
C32 0.22u
C190 1u
C191 10u
VCC1P2 ENET_DVDDL
L7 60ohm 3A
C30 0.22u
C48 1u
C29 10u
Copyright (c) 2013 by Terasic Technologies Inc. Taiwan.
All rights reserved.
No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.
Title
DE1-SoC Board
Size B
Document Number
1 Gagabit Ethernet
Rev C
Date: Monday, March 24, 2014
Sheet 23 of 30



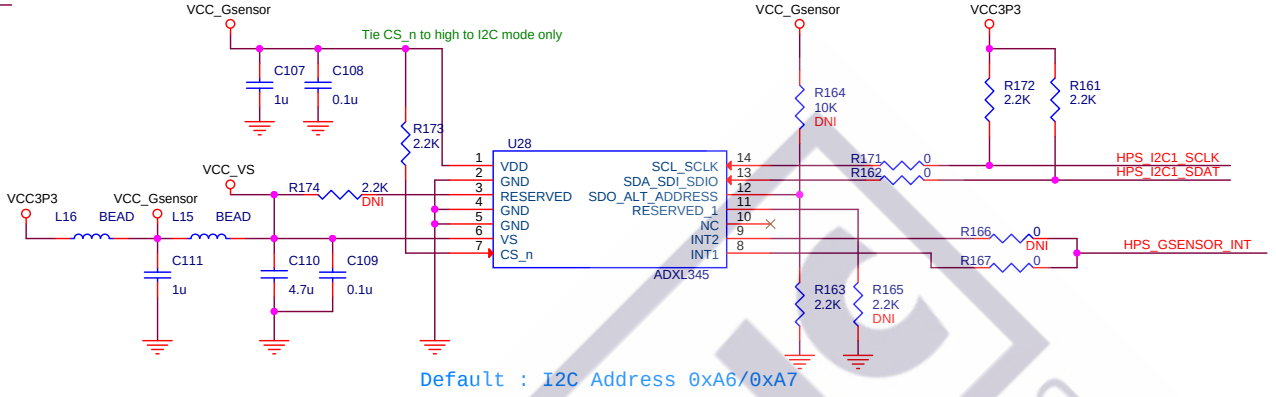
Title: **DE1-SoC Board**

Size	Document Number	Rev
B	UART to USB, SD CARD	C

Date: Monday, March 24, 2014 Sheet 24 of 30

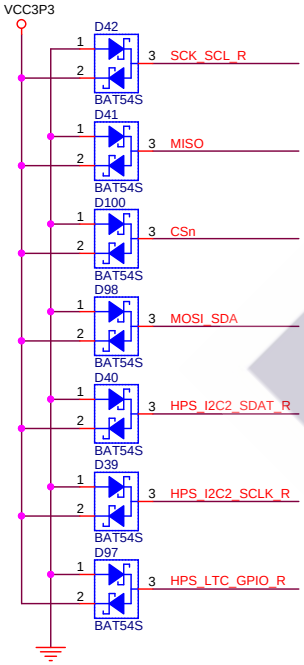
HPS_I2C1_SDAT 5,26
HPS_I2C1_SCLK 5,26
HPS_GSENSOR_INT 5

Digital Accelerometer

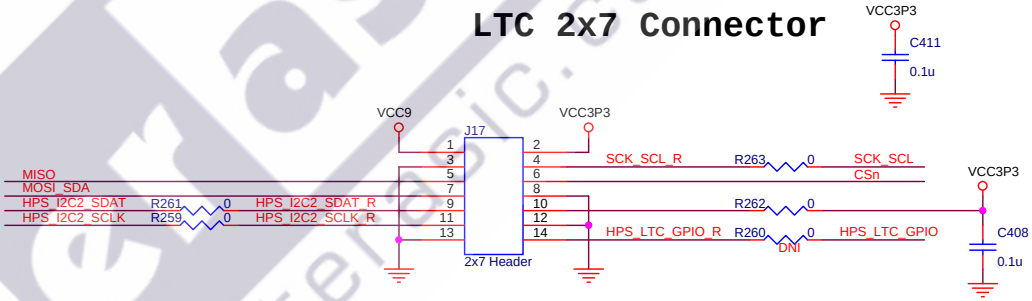


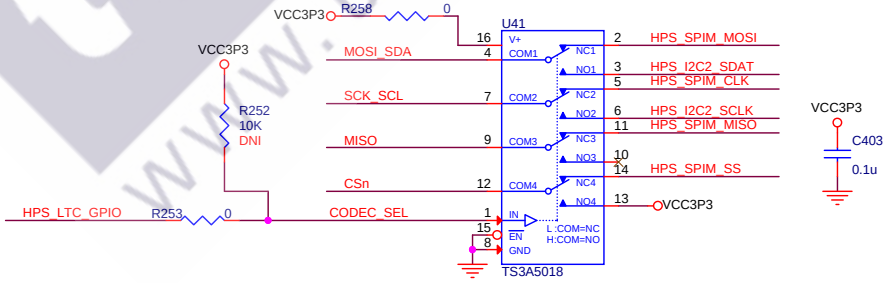
Default : I2C Address 0xA6/0xA7

HPS_I2C2_SCLK 5
HPS_I2C2_SDAT 5
HPS_SPIM_MOSI 5
HPS_SPIM_CLK 5
HPS_SPIM_SS 5
HPS_SPIM_MISO 5
HPS_LTC_GPIO 5



LTC 2x7 Connector

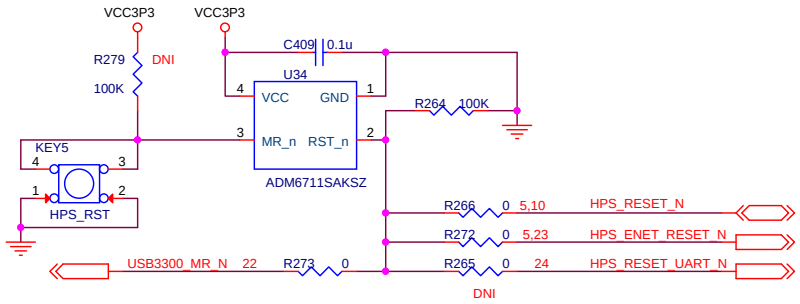




Title: **DE1-SoC Board**

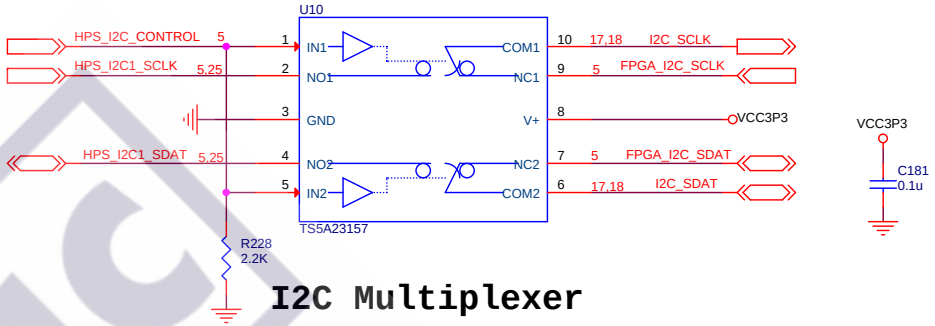
Size	Document Number	Rev
B	Accelerometer, LTC Connector	C

Date: Monday, March 24, 2014 Sheet 25 of 30

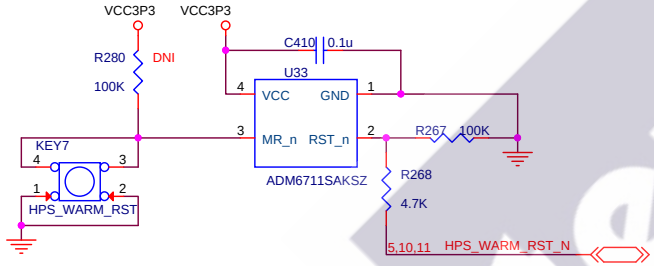


HPS Cold Reset

LOW --> NC to/from COM = ON and NO to/from COM = OFF
HIGH --> NC to/from COM = OFF and NO to/from COM = ON

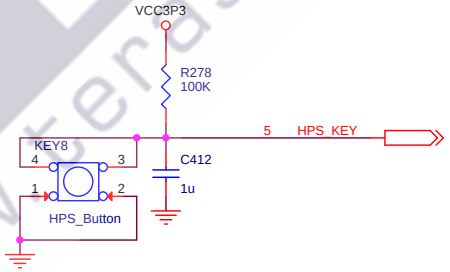


I2C Multiplexer



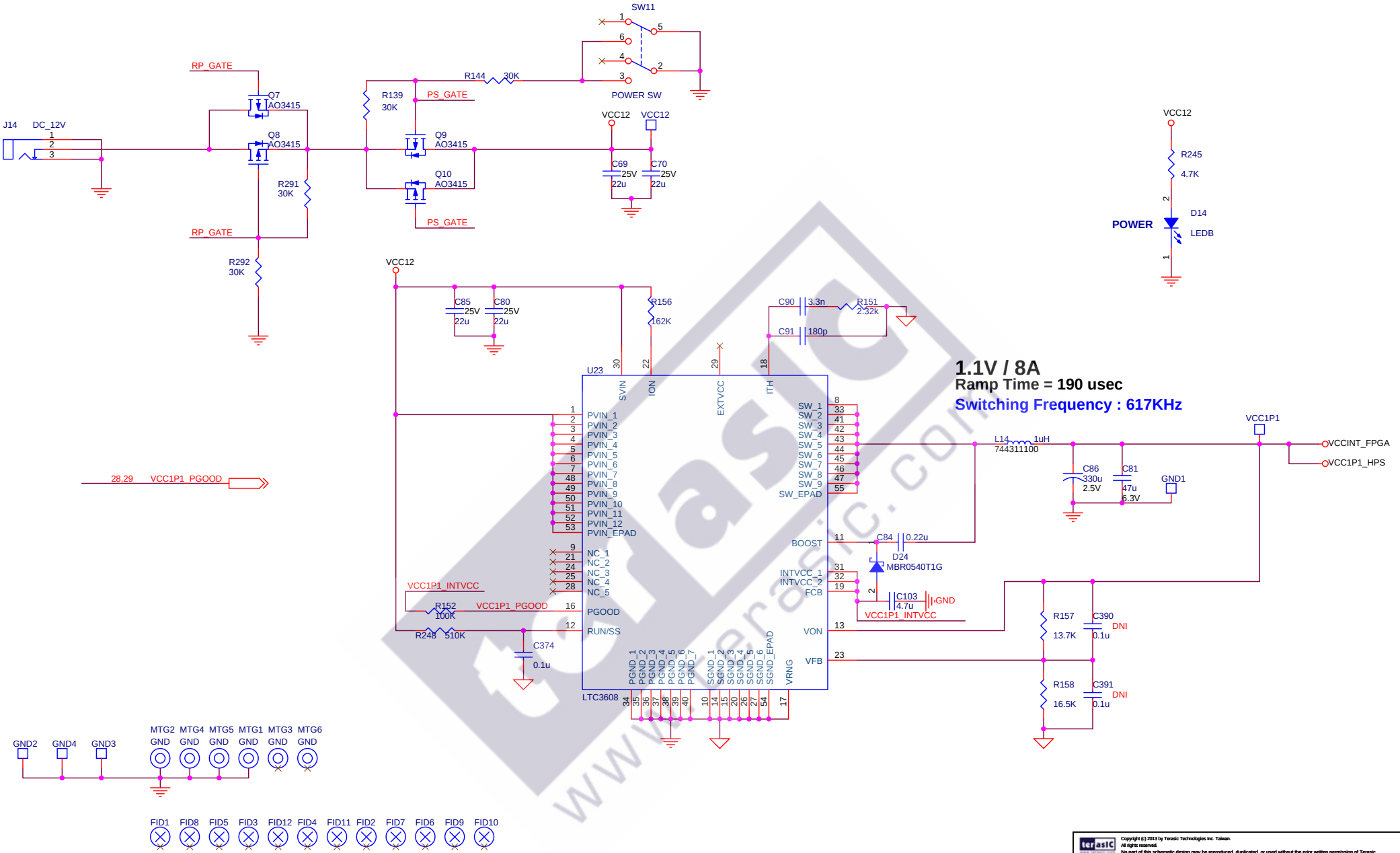
HPS Warm Reset

HPS User LED



HPS User Button

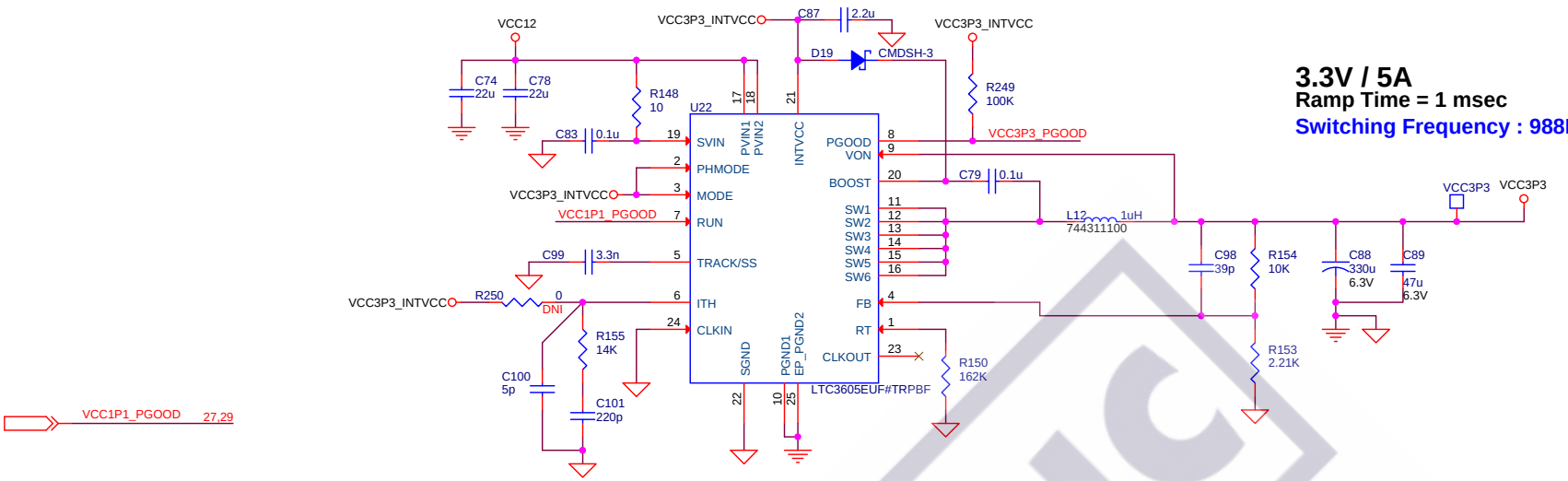
Title	DE1-SoC Board	
Size B	Document Number I2C Multiplexer, HPS BUTTON, HPS LED	Rev C
Date: Monday, March 24, 2014	Sheet 26 of 30	



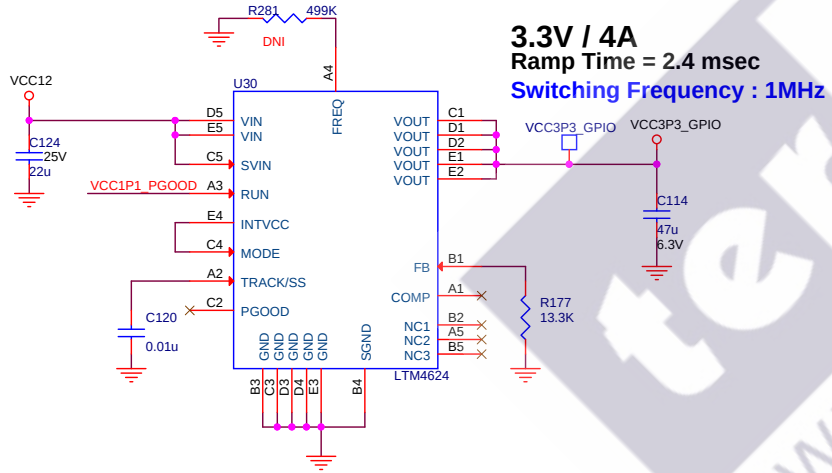
Title: **DE1-SoC Board**

Size	Document Number	Rev
B	Power - 1.1V	C

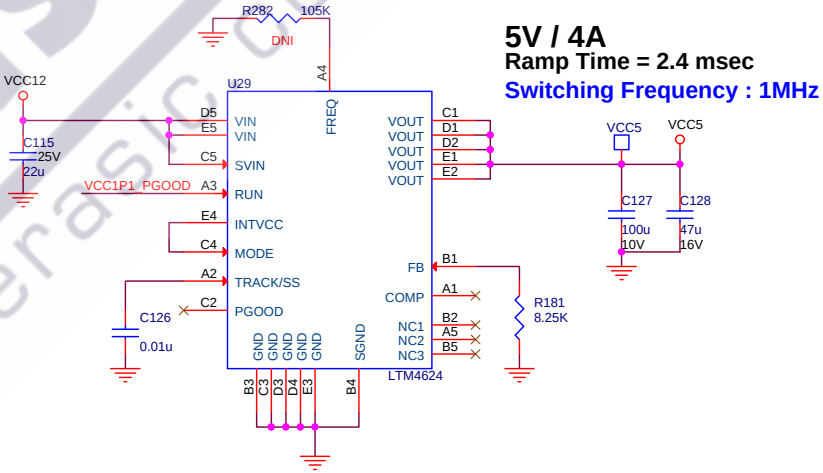
Date: Monday, March 24, 2014 Sheet 27 of 30



3.3V / 5A
Ramp Time = 1 msec
Switching Frequency : 988KHz



3.3V / 4A
Ramp Time = 2.4 msec
Switching Frequency : 1MHz

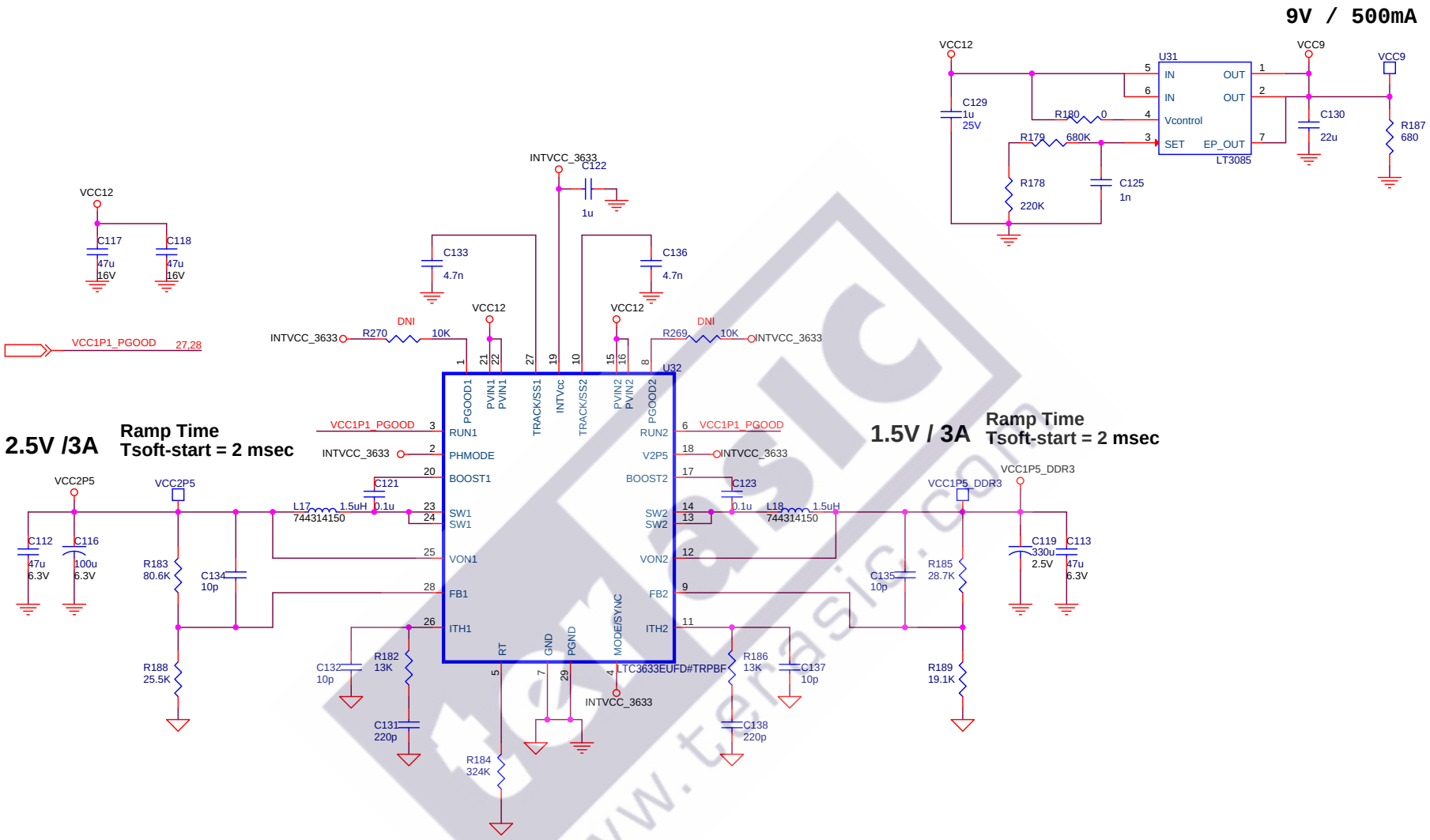


5V / 4A
Ramp Time = 2.4 msec
Switching Frequency : 1MHz

Title: **DE1-SoC Board**

Size	Document Number	Rev
B	Power - 5V, 3.3V	C

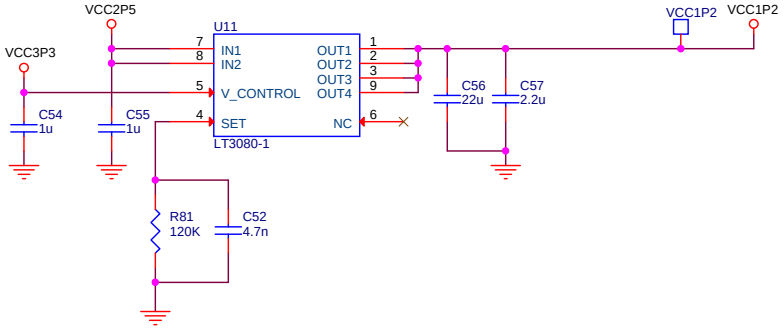
Date: Monday, March 24, 2014 Sheet 28 of 30



Title	DE1-SoC Board	
Size B	Document Number Power - 9V, 2.5V, 1.5V	Rev C
Date: Monday, March 24, 2014	Sheet 29 of 30	

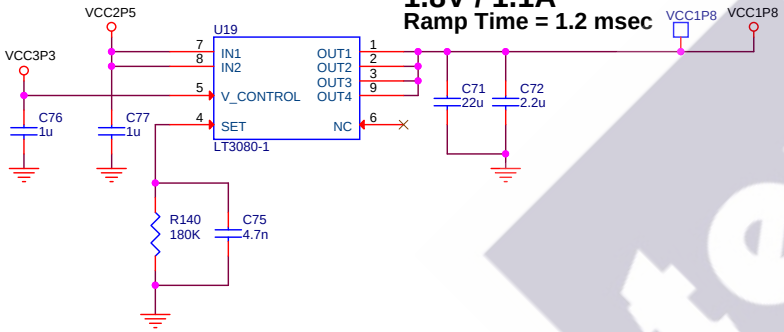
1.2V / 1.1A

Ramp Time = 0.8msec

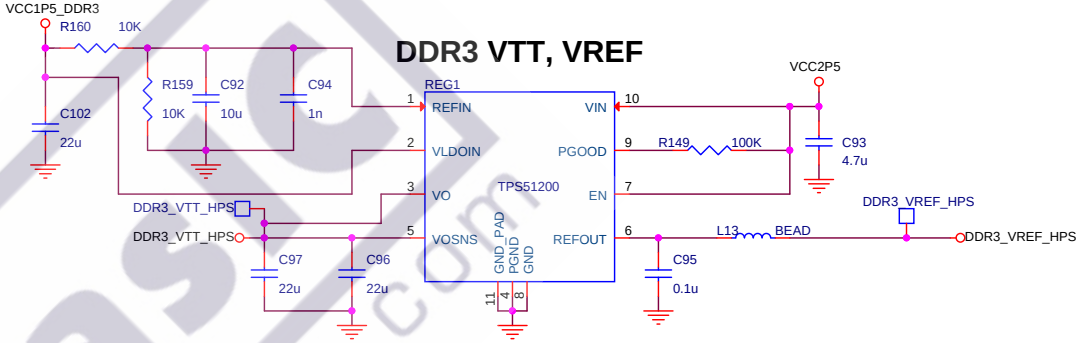


1.8V / 1.1A

Ramp Time = 1.2 msec



DDR3 VTT, VREF



Title	DE1-SoC Board	
Size B	Document Number: Power - 1.2V, 1.8V, DDR3 VREF, DDR3 VTT	Rev C
Date: Monday, March 24, 2014	Sheet 30 of 30	