    - Optional register lockdown on some group 0 interrupts.
- CPU private registers have restricted accessed on the AXI interconnect.

GIC Proxy Interrupts

The GIC proxy manages all the system interrupts connected to the GIC SPI interrupts. These system interrupts set bits in the GICP{0:4}_IRQ_STATUS registers. After the masking registers, the bit in each register is OR'ed together to set bits in another status register that is OR'ed together to generate a single interrupt signal to the PMU external interrupt controller.

The GIC proxy interrupts are used by the PMU in a fall-back mode to handle system interrupts that cannot be managed by the application processors.

System Interrupts

The system interrupts are generated by many system elements and broadcast to the GICs, the PMU via the GIC proxy (GICPx_IRQ registers), and to output signals in the PL. The system interrupts are listed in Table 13-1. The table lists the IRQ numbers for the RPU and APU interrupt controllers, as well as the GIC proxy bit assignments.

Table 13-1: **System Interrupts**

IRQ Name	IRQ Number (GIC)	GICPx_IRQ Bits (GIC Proxy)	Description
RPU0_Perf_Mon	40	GICP0 [8]	RPU0 performance monitor (ARM_PMU)(1).
RPU1_Perf_Mon	41	GICP0 [9]	RPU1 performance monitor (ARM_PMU)(1).
OCM	42	GICP0 [10]	OCM CE and UE ECC errors.
LPD_APB	43	GICP0 [11]	OR of all APB slave interface errors in LPD.
RPU0_ECC	44	GICP0 [12]	RPU0 CE and UE ECC errors.
RPU1_ECC	45	GICP0 [13]	RPU1 CE and UE ECC errors.
NAND	46	GICP0 [14]	NAND memory controller.
QSPI	47	GICP0 [15]	Quad-SPI controller.
GPIO	48	GICP0 [16]	GPIO controller.
I2C0	49	GICP0 [17]	I2C0 controller.
I2C1	50	GICP0 [18]	I2C1 controller.
SPI0	51	GICP0 [19]	SPI0 controller.
SPI1	52	GICP0 [20]	SPI1 controller.
UART0	53	GICP0 [21]	UART 0 controller.
UART1	54	GICP0 [22]	UART 1 controller.

Table 13-1: **System Interrupts *(Cont'd)***

IRQ Name	IRQ Number (GIC)	GICPx_IRQ Bits (GIC Proxy)	Description
CAN0	55	GICP0 [23]	CAN 0 controller.
CAN1	56	GICP0 [24]	CAN 1 controller.
LPD_APM	57	GICP0 [25]	OR of the LPD and OCM APM interrupts.
RTC_Alarm	58	GICP0 [26]	RTC alarm interrupt.
RTC_Seconds	59	GICP0 [27]	RTC seconds interrupt.
ClkMon	60	GICP0 [28]	Clock monitor in LPD.
IPI_Ch7	61	GICP0 [29]	IPIs targeting channel 7.
IPI_Ch8	62	GICP0 [30]	IPIs targeting channel 8.
IPI_Ch9	63	GICP0 [31]	IPIs targeting channel 9.
IPI_Ch10	64	GICP1 [0]	IPIs targeting channel 10.
IPI_Ch1	65	GICP1 [1]	IPIs targeting channel 1.
IPI_Ch2	66	GICP1 [2]	IPIs targeting channel 2.
IPI_Ch0	67	GICP1 [3]	IPIs targeting channel 0.
TTC0	68:70	GICP1 [4:6]	Triple-timer counter 0.
TTC1	71:73	GICP1 [7:9]	Triple-timer counter 1.
TTC2	74:76	GICP1 [10:12]	Triple-timer counter 2.
TTC3	77:79	GICP1 [13:15]	Triple-timer counter 3.
SDIO0	80	GICP1 [16]	SDIO 0 controller.
SDIO1	81	GICP1 [17]	SDIO 1 controller.
SDIO0_Wakeup	82	GICP1 [18]	SDIO 0 wake-up interrupt.
SDIO1_Wakeup	83	GICP1 [19]	SDIO 1 wake-up interrupt.
LPD_SWDT	84	GICP1 [20]	LPD watchdog timer (wdt0). Edge sensitive trigger.(2)
CSU_SWDT	85	GICP1 [21]	CSU and PMU watchdog timer. Edge sensitive trigger.(2)
LPD_ATB	86	GICP1 [22]	OR of all ATB timeout errors in LPD.
AIB	87	GICP1 [23]	OR of all AIB errors on AXI and APB.
SysMon	88	GICP1 [24]	OR of all system monitor interrupts.
GEM0	89	GICP1 [25]	Ethernet 0 controller.
GEM0_Wakeup	90	GICP1 [26]	Ethernet 0 wake-up interrupt.
GEM1	91	GICP1 [27]	Ethernet 1 controller.
GEM1_Wakeup	92	GICP1 [28]	Ethernet 1 wake-up interrupt.
GEM2	93	GICP1 [29]	Ethernet 2 interrupt.
GEM2_Wakeup	94	GICP1 [30]	Ethernet 2 wake-up interrupt.
GEM3	95	GICP1 [31]	Ethernet 3 controller.