Register and Buffer Summary

The IPI interrupt channels and message buffers are pre-defined and software associated as described in Table 13-3.

Note: The software might reassign the interrupt channels and message buffers except for the PMU interrupts.

Table 13-3: **IPI Channel and Message Buffer Default Associations**

Channel Number	Default Owner	IPI Interrupt Registers			IPI Message Buffers		
		Name	Base Address	XPPU 64 KB Aperture	SI Agent Number	Base Address	XPPU 32B Apertures
Channel 0	APU MPSoC	Channel0	0xFF30_0000	048	1	0xFF99_0000	256 - 271
Channel 1	RPU0	Channel1	0xFF31_0000	049	2	0xFF99_0200	272 - 287
Channel 2	RPU1	Channel2	0xFF32_0000	050	3	0xFF99_0400	288 - 303
Channel 3	PMU(1)	PMU_0(2)	0xFF33_0000	051	8	0xFF99_0E00	368 - 383
Channel 4		PMU_1	0xFF33_1000				
Channel 5		PMU_2	0xFF33_2000				
Channel 6		PMU_3	0xFF33_3000				
Channel 7	PL 0	Channel7	0xFF34_0000	052	4	0xFF99_0600	304 - 319
Channel 8	PL 1	Channel8	0xFF35_0000	053	5	0xFF99_0800	320 - 335
Channel 9	PL 2	Channel9	0xFF36_0000	054	6	0xFF99_0A00	336 - 351
Channel 10	PL 3	Channel10	0xFF37_0000	055	7	0xFF99_0C00	352 - 367

Notes:
1. The PMU interrupts are hardwired because the PMU IRQ signals only go to the PMU interrupt.
2. The PMI IPI0 interrupt causes the PMU to enter sleep mode.

Programming

The communication channels between processors must be coordinated with an agreed upon protocol and message format.

Generate an Interrupt

To generate an interrupt, the sender writes a 1 to a bit in its trigger (TRIG) register that corresponds to the target receiver. It can verify that a bit is set in the receiver's status register by reading its own OBS register. However, it cannot determine if the interrupt is enabled to generate the IRQ interrupt signal.